Design of Stable and Precise Closed-Loop Interfaces for PHIL Applications

Systematic Approaches

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Outline

Interface problematic

Importance of closing the loop

- PHIL testing today is largely Device Under Test (DUT) oriented
- From utilities' perspective it is more important to test DUT-grid interactions
- Requires two key elements
  - High fidelity power amplifier (PA)
  - **Robustly stable and transparent closed-loop interface**

Definitions and challenges

- **PHIL interface:** a set of signals and measurements exchanged between an ROS model simulated in RT and a power amplifier (PA) connected to a physical DUT
- **Robust stability:** must ensure stable closed-loop operation for (ideally) any ROS and DUT
- Closed-loop **transparency:** minimum dynamics introduced to the PHIL simulation
- The two objectives are generally conflicting

PHIL interface methods: an overview

Method	Limitations
ITM and modifications	Stability depends on ROS and DUT impedance ratio, requires filtering or DQ frame, which limit bandwidth
DIM and other DUT estimation-based methods	Require knowledge of DUT to design damping impedance, thus not robust to DUT perturbations
PCD and circuit relaxation-based methods	Stability guaranteed with convergence of fixed-point iterations, which is not possible in PHIL
Transmission Line Interface (TLI) method	Theoretical robust stability guarantees due to passivity, requires **robust impedance emulation**
Optimal control approaches	Robustness guarantees for bounded uncertainty

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Systematic interface design via optimal and robust control methods

Why optimal (robust) control?

- Formulate interface design as an optimization problem
- Stability and performance are **systematically handled together** within the design procedure
- Several ways to approach robust stability
  - Incorporate ROS and DUT variations as uncertainties – design methodologies with guarantees
  - Passivity as design criterion
- Numerical efficiency when reduced to convex problems
  - Powerful commerical solvers

Challenges

- PHIL interface is a hybrid discrete/continuous system – hard to model for synthesis
- Often use distributed CPU/FPGA interface architecture that imposes a certain structure
  - Breaks convexity of synthesis
- Currently available robust stability design methods only work for bounded uncertainty model – not suitable for extreme scenarios, e.g., open- and short-circuit conditions
- Performance specifications are defined for frequency ranges, rather than for all frequencies
  - Some can be handled using appropriate weight selection
  - Others, like passivity, require new design methods and algorithms

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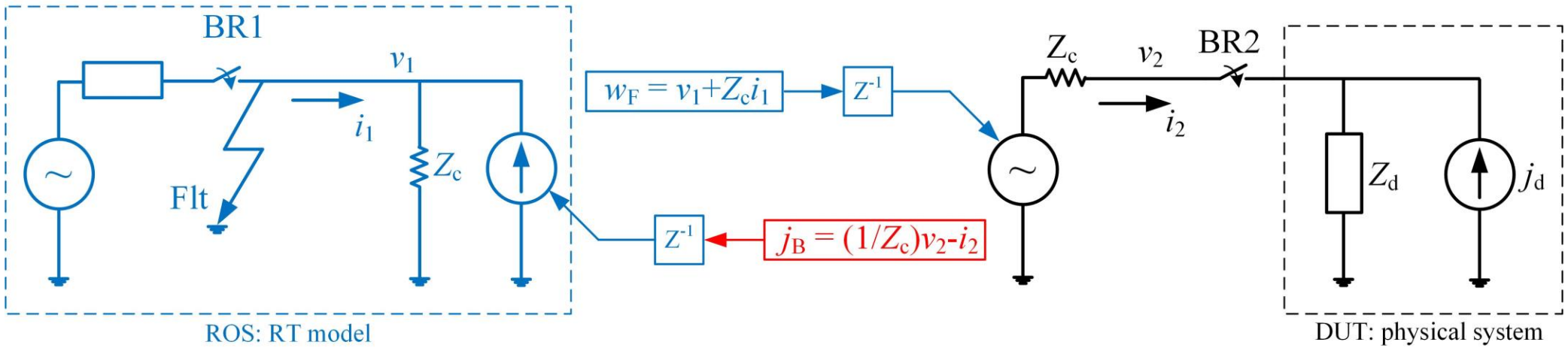
Application example

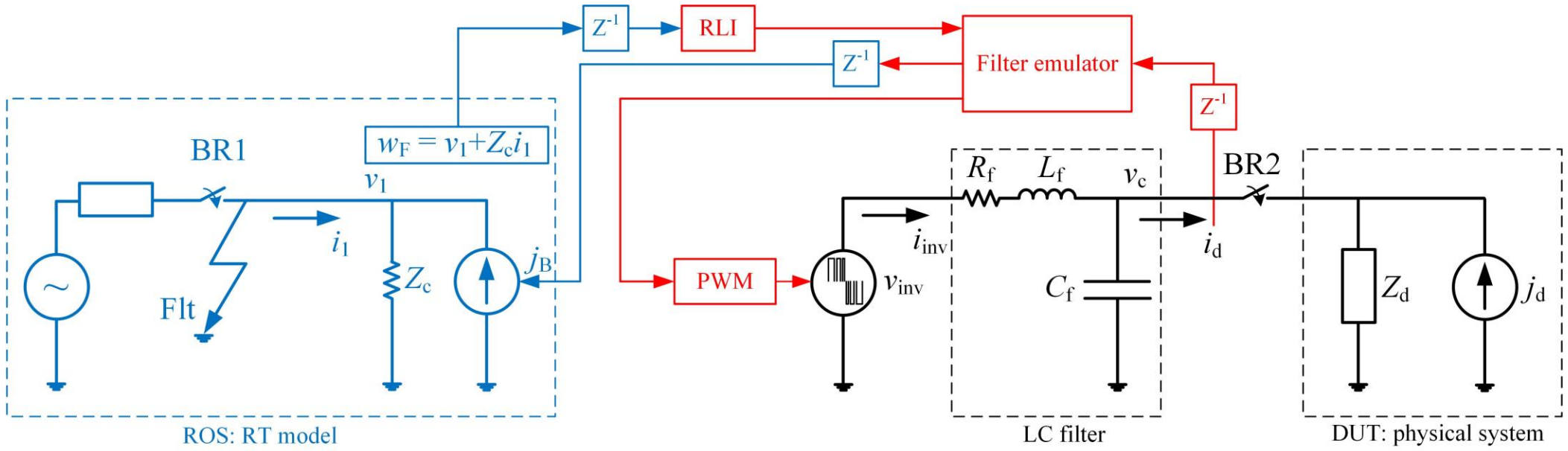
TLI method and impedance emulation problem



- Very stable but lacks transparency
  - Useful trick – use existing line of the ROS model as interface
- Requires a resistor at the PA output to properly model the characteristic impedance (CI) of a transmission line – **not feasible in practice**
  - Large losses if CI is large
  - PA needs to be oversized to generate large voltages
  - Physical manipulations are required if CI is changed

TLI method and impedance emulation problem

- IREQ solution: emulate the presence of CI via a fast (FPGA) control loop (“Filter emulator”, FE)

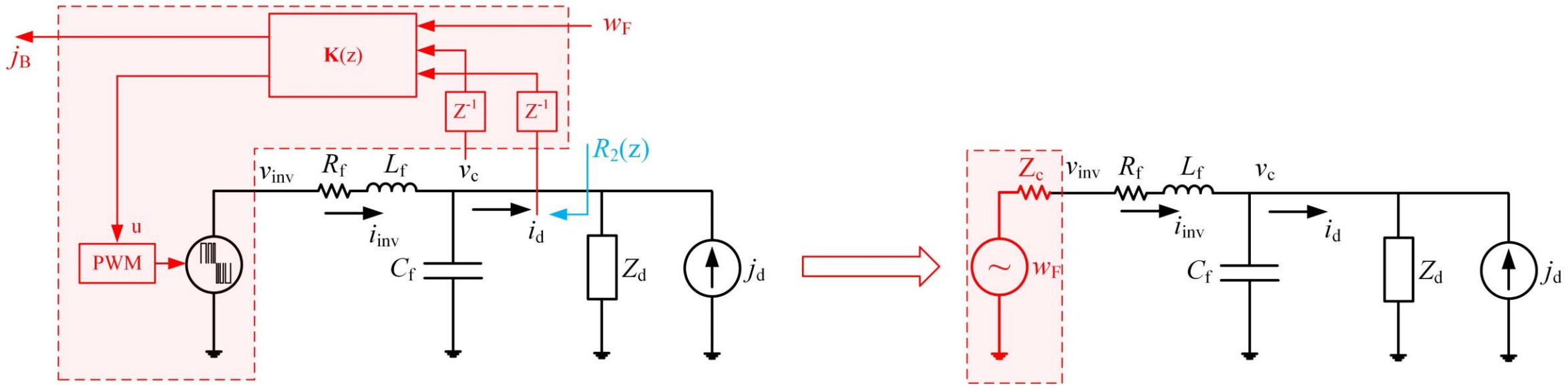


TLI method and impedance emulation problem

- FE – open loop observer, generates control signal and provides estimate of $\boldsymbol{i_{inv}}$ for backward wave calculation
- Identified stability issues in the conditions of low impedance DUT
  - Not an issue for the 3 kW IREQ testbed (switch and PCB losses provide damping)
  - Problematic for the 25-kV, 7.5-MVA PHIL application, resistive damping would require a cooling system

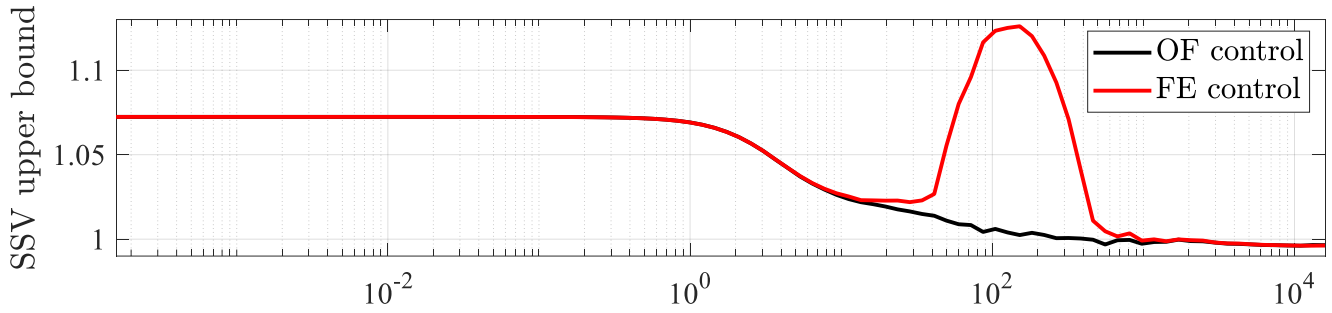
Improving stability of TLI method

- Solution: systematically design robust impedance emulation control loop
  - Use H_∞ synthesis, formulate as Optimal Filter (OF) problem

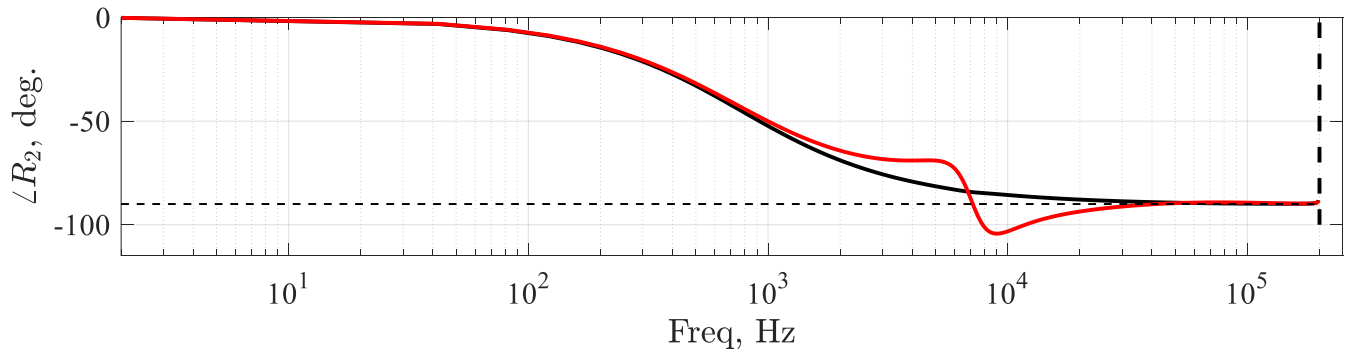


Robust stability of impedance emulation loop

- For this application not enforced by design but checked a posteriori using two approaches
  - μ-analysis for uncertain Z_d



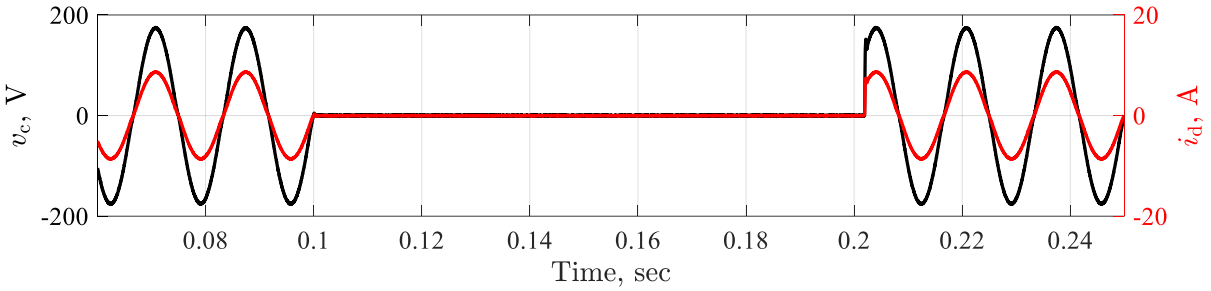
- Passivity of the impedance seen by the DUT



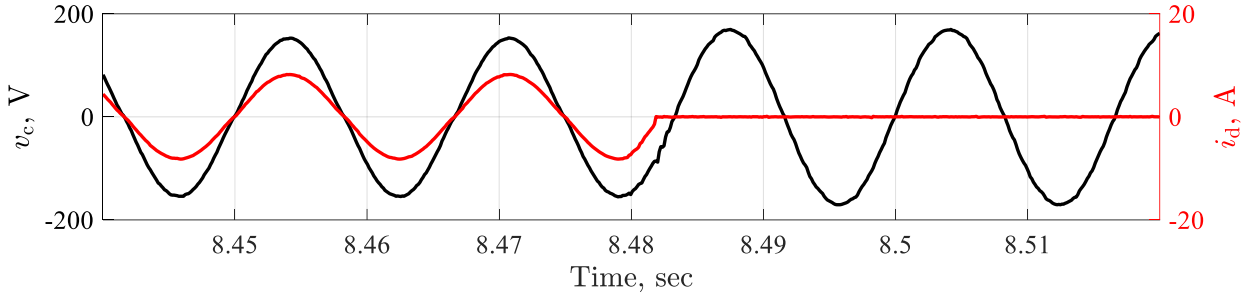
IREQ testbed: experimental results

- PHIL transients with resistive load and inverter

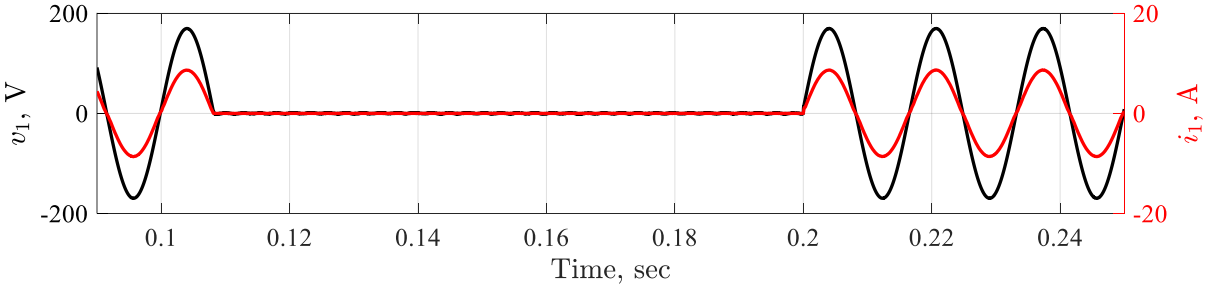
ROS short-circuit, resistive load



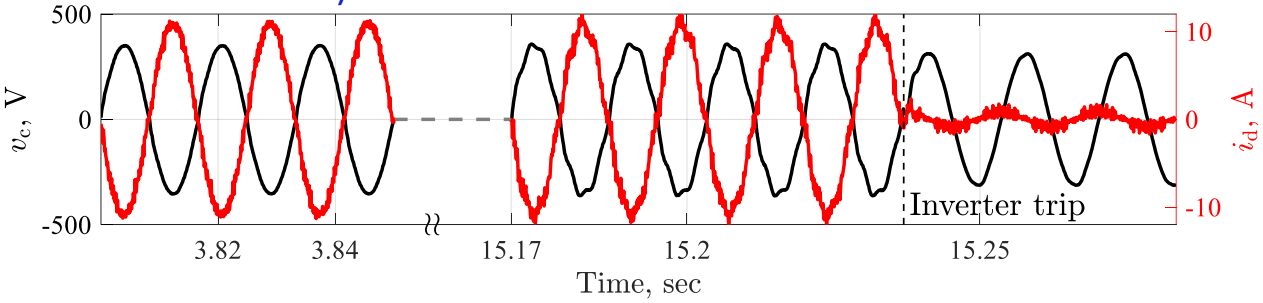
DUT open circuit, resistive load



ROS open circuit, resistive load



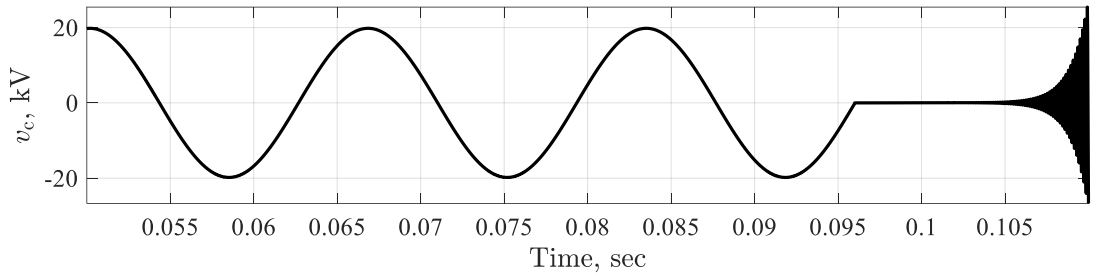
Solar inverter test following SCL change (300 kVA -> 90 KVA)



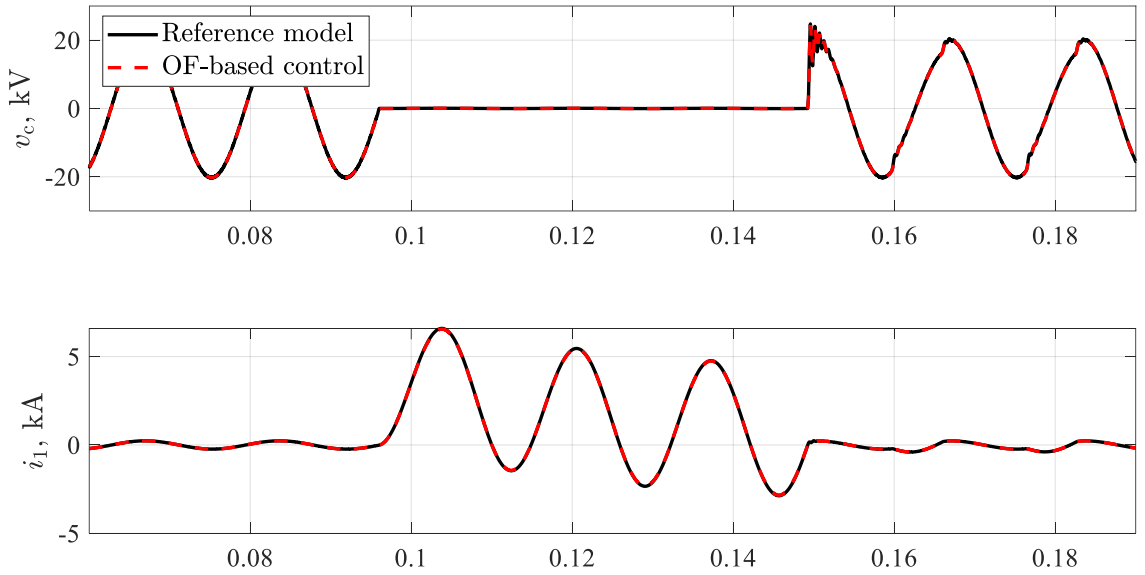
Large-scale PHIL: simulation results

- DUT short-circuit fault – extreme scenario (PA will likely trip anyway) but demonstrates shortcomings of FE
- Similar scenario – strong source on DUT side (e.g., grid-forming inverter)

FE performance



OF performance



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Conclusions and research directions

Concluding remarks

- Closing the loop is still an open problem
- Not a general solution, but instead a case-by-case approach determined by a system to be tested
- Systematic methods are even more important in this context
  - Subject of collaboration between IREQ, OPAL-RT and McGill University
- Resulting solutions are implementable in practice

Future research

- Adapting systematic methods from control theory to interface design problem is a great first step, but limitations exist
- Need to develop new synthesis procedures that can handle PHIL related limitations
  - structural constraints
  - extreme circuit conditions
  - finite frequency specifications
- Systematic interface design methods require ROS, DUT and PA knowledge to some degree
  - Need system identification methods when no models are available

Stable and precise interface techniques allow for complex CP-HIL tests for various grid configurations

- Transmission, distribution, isolated grids and microgrids
- Enable in-depth testing of new technologies, e.g., GFM inverters – subject of on-going work supported by NRCAN

Thank you! Questions?