

Improving Power Hardware-in-the-loop Interfaces via Optimal Control

Jonathan Eid, Ashley Meagher

McGill University, Department of Mechanical Engineering



McGill

DECAR



OPAL-RT
TECHNOLOGIES



17 June 2026

The Power Hardware-in-the-loop Interfacing Problem

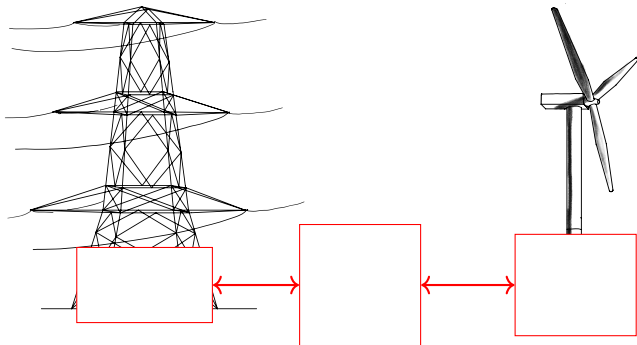
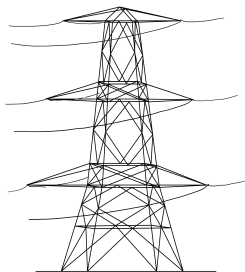
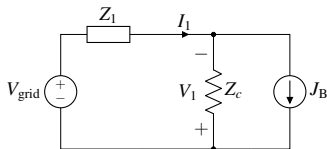


Figure 1: Power hardware-in-the-loop (PHIL) simulation.

The Power Hardware-in-the-loop Interfacing Problem



(a) Illustration of the simulated grid.



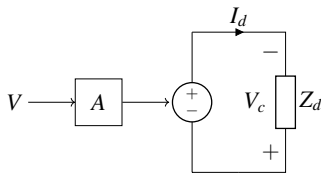
(b) Circuit model of the simulated grid.

Figure 2: The simulated grid.

The Power Hardware-in-the-loop Interfacing Problem



(a) Illustration of the device.



(b) Circuit model of the amplifier and device.

Figure 3: The amplifier and device under test.

The Power Hardware-in-the-loop Interfacing Problem

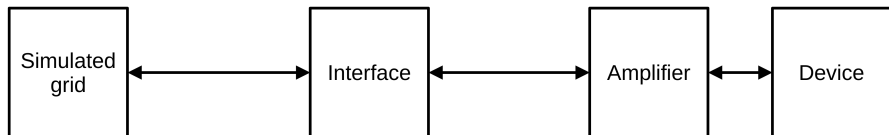


Figure 4: Illustration of a PHIL experimental setup.

The Power Hardware-in-the-loop Interfacing Problem

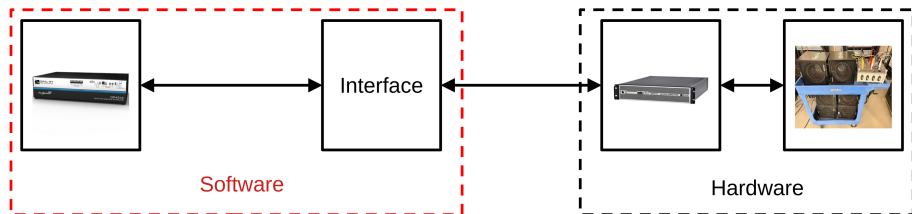
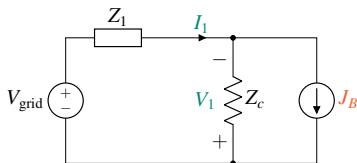


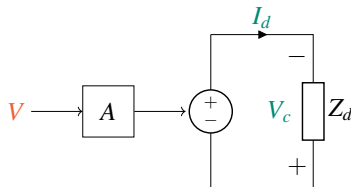
Figure 5: Illustration of a PHIL experimental setup.

¹ Images retrieved from <https://tmesystems.net/RT-LAB>,
<https://www.opal-rt.com/hardware/simulators/real-time-simulators/op4512/>,
and <https://opal-rt.atlassian.net/wiki/spaces/PSSDD/pages/144647230/OP8110+4Q+Power+Amplifier>.

The Power Hardware-in-the-loop Interfacing Problem



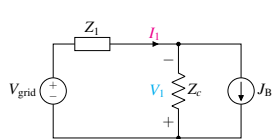
(a) Circuit model of the simulated grid.



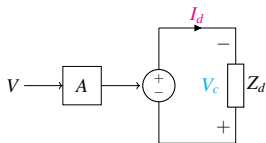
(b) Circuit model of the amplifier and device.

Stable interface: the measurement signals, V_1 , I_1 , V_c , and I_d , and actuation signals, V and J_B , do not diverge.

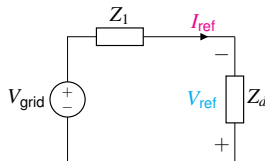
The Power Hardware-in-the-loop Interfacing Problem



(a) Circuit model of the simulated grid.



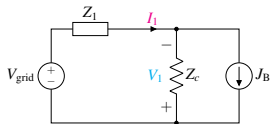
(b) Circuit model of the amplifier and device.



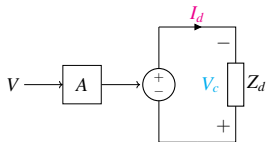
(c) Circuit model of the idealized interconnection.

Two notions of **precision**: accuracy and transparency.

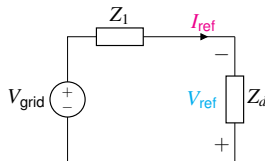
The Power Hardware-in-the-loop Interfacing Problem



(a) Circuit model of the simulated grid.



(b) Circuit model of the amplifier and device.

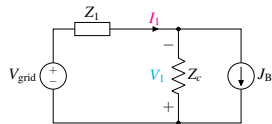


(c) Circuit model of the idealized interconnection.

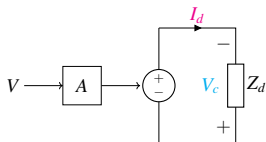
Two notions of **precision**: accuracy and transparency.

Accurate interface: the signals $V_1 - V_c$ and $I_1 - I_d$ converge to zero.

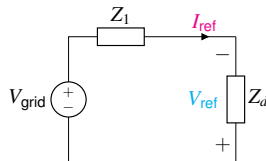
The Power Hardware-in-the-loop Interfacing Problem



(a) Circuit model of the simulated grid.



(b) Circuit model of the amplifier and device.



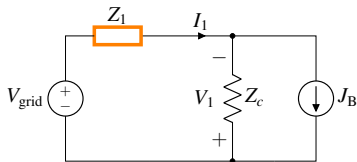
(c) Circuit model of the idealized interconnection.

Two notions of **precision**: accuracy and transparency.

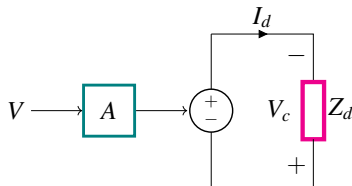
Accurate interface: the signals $V_1 - V_c$ and $I_1 - I_d$ converge to zero.

Transparent interface: the signals $V_1 - V_{\text{ref}}$, $V_c - V_{\text{ref}}$, $I_1 - I_{\text{ref}}$, and $I_d - I_{\text{ref}}$ converge to zero.

The Power Hardware-in-the-loop Interfacing Problem



(a) Off-nominal circuit model of the simulated grid.

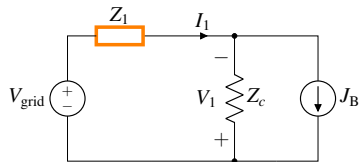


(b) Off-nominal circuit model of the amplifier and device.

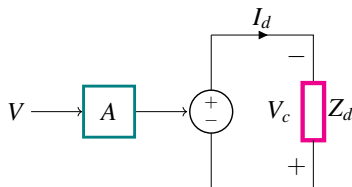
Practical PHIL experiments involve

- communication **delays**,

The Power Hardware-in-the-loop Interfacing Problem



(a) Off-nominal circuit model of the simulated grid.

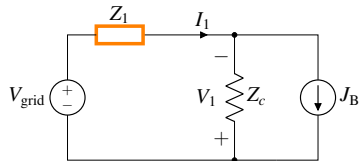


(b) Off-nominal circuit model of the amplifier and device.

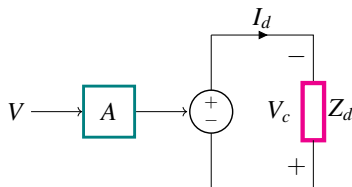
Practical PHIL experiments involve

- ▶ communication **delays**,
- ▶ intentional **variation** of the **grid load**,

The Power Hardware-in-the-loop Interfacing Problem



(a) Off-nominal circuit model of the simulated grid.

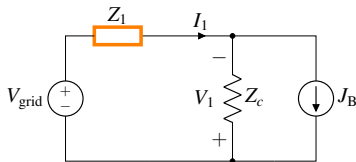


(b) Off-nominal circuit model of the amplifier and device.

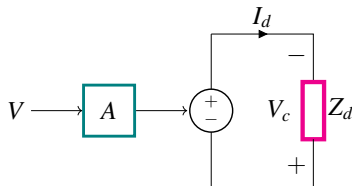
Practical PHIL experiments involve

- ▶ communication **delays**,
- ▶ intentional **variation** of the **grid load**,
- ▶ **uncertainties** in **amplifier model** due to system identification, and

The Power Hardware-in-the-loop Interfacing Problem



(a) Off-nominal circuit model of the simulated grid.

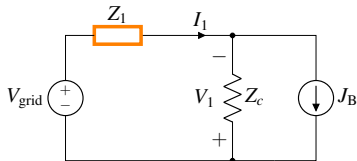


(b) Off-nominal circuit model of the amplifier and device.

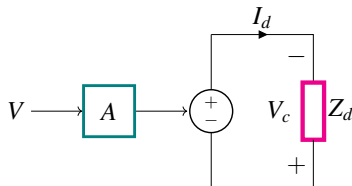
Practical PHIL experiments involve

- ▶ communication **delays**,
- ▶ intentional **variation** of the **grid load**,
- ▶ **uncertainties** in **amplifier model** due to system identification, and
- ▶ **uncertainties** in and **various operating conditions** of **device load** due to linear model approximating complex hardware.

The Power Hardware-in-the-loop Interfacing Problem



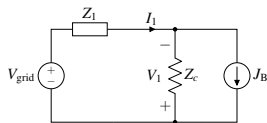
(a) Off-nominal circuit model of the simulated grid.



(b) Off-nominal circuit model of the amplifier and device.

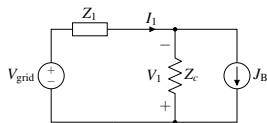
Robust interface: stability is ensured even under uncertainties and various operating conditions.

Approach to Precision: Model Matching

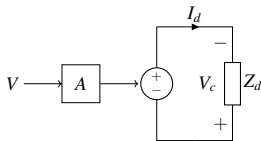


(a) ROS model.

Approach to Precision: Model Matching

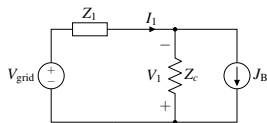


(a) ROS model.

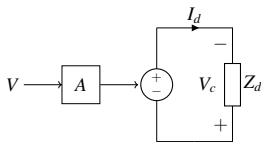


(b) DUT and amplifier models.

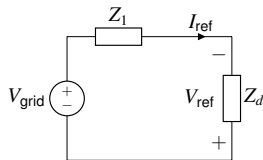
Approach to Precision: Model Matching



(a) ROS model.

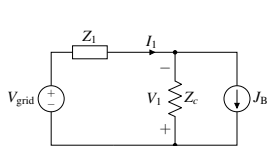


(b) DUT and amplifier models.

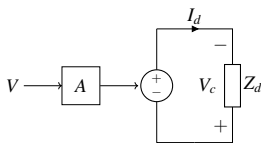


(c) Idealized, reference interconnection.

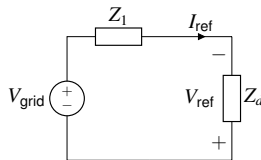
Approach to Precision: Model Matching



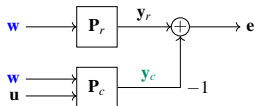
(a) ROS model.



(b) DUT and amplifier models.

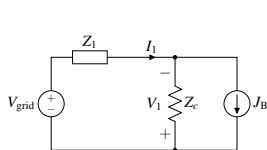


(c) Idealized, reference interconnection.

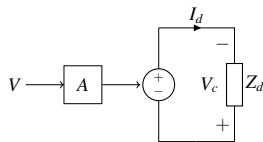


(d) Model matching architecture, where $\mathbf{z} = [\mathbf{e}^T \mathbf{u}^T]^T$ and $\mathbf{y} = \mathbf{y}_c$.

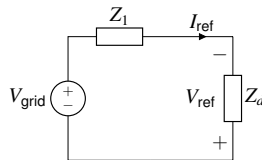
Approach to Precision: Model Matching



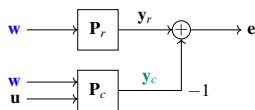
(a) ROS model.



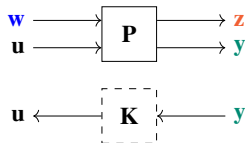
(b) DUT and amplifier models.



(c) Idealized, reference interconnection.



(d) Model matching architecture, where $\mathbf{z} = [\mathbf{e}^T \mathbf{u}^T]^T$ and $\mathbf{y} = \mathbf{y}_c$.



(e) Generalized control problem.

Experimental Validation

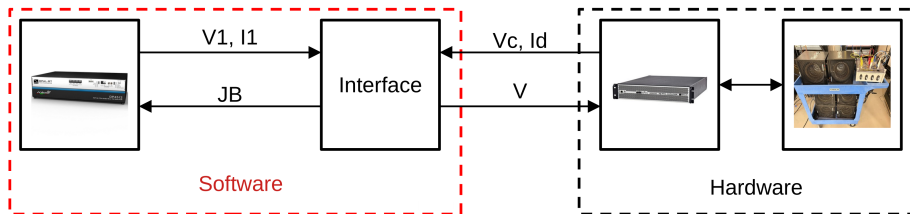
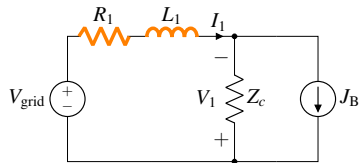


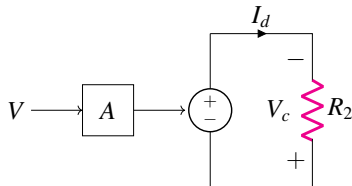
Figure 11: Illustration of a PHIL experimental setup.

¹ Images retrieved from <https://tmesystems.net/RT-LAB>,
<https://www.opal-rt.com/hardware/simulators/real-time-simulators/op4512/>,
and <https://opal-rt.atlassian.net/wiki/spaces/PSSDD/pages/144647230/OP8110+4Q+Power+Amplifier>.

Experimental Validation

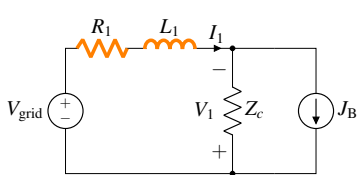


(a) Experiment-specific model of the simulated grid.

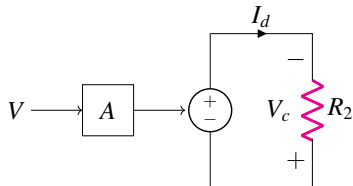


(b) Experiment-specific model of the device.

Experimental Validation



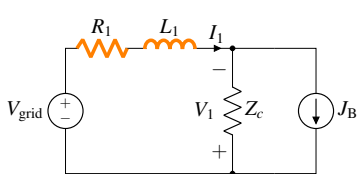
(a) Experiment-specific model of the simulated grid.



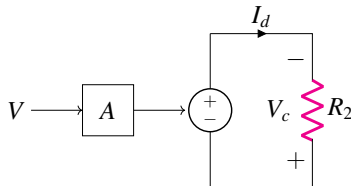
(b) Experiment-specific model of the device.

The **device** is modeled as a resistor.

Experimental Validation



(a) Experiment-specific model of the simulated grid.

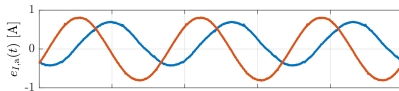
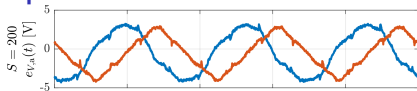


(b) Experiment-specific model of the device.

The **device** is modeled as a resistor.

The **grid load** is modeled as a resistor and inductor inversely proportional to the grid's *short-circuit ratio* S .

Experimental Validation



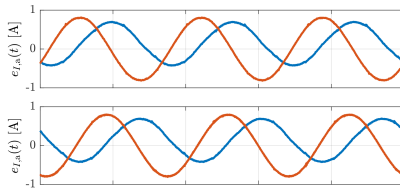
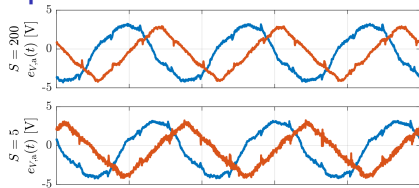
Time, t [s]

Time, t [s]

— $\mathcal{H}_\infty$ MM — ITM

Figure 13: Time-domain response comparison of an $\mathcal{H}_\infty$ model matching-based and ITM-based interface under various operating conditions.

Experimental Validation



Time, t [s]

Time, t [s]

— $\mathcal{H}_\infty$ MM — ITM

Figure 14: Time-domain response comparison of an $\mathcal{H}_\infty$ model matching-based and ITM-based interface under various operating conditions.

Experimental Validation

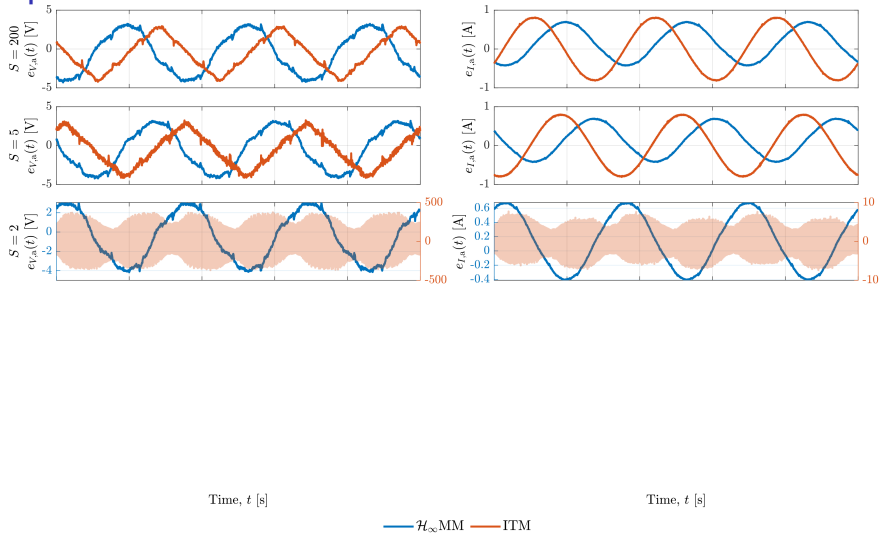


Figure 15: Time-domain response comparison of an $\mathcal{H}_\infty$ model matching-based and ITM-based interface under various operating conditions.

Experimental Validation

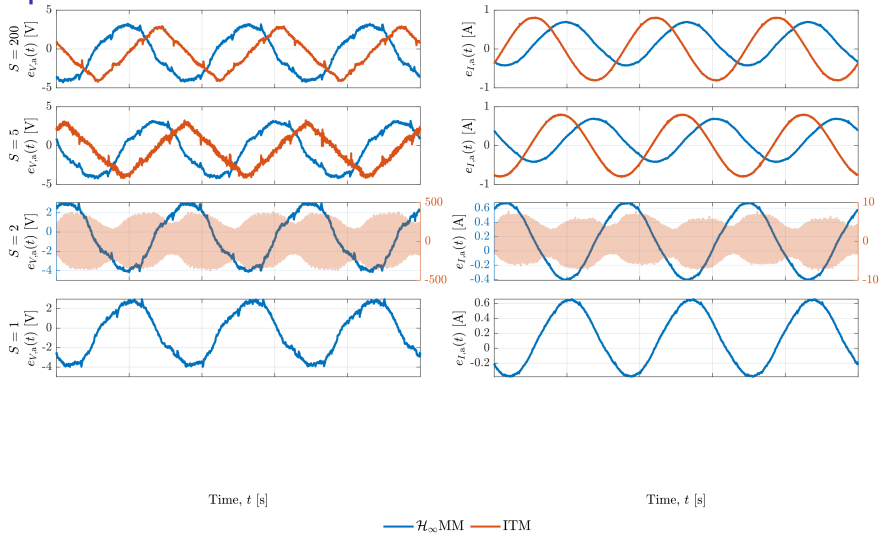


Figure 16: Time-domain response comparison of an $\mathcal{H}_\infty$ model matching-based and ITM-based interface under various operating conditions.

Experimental Validation

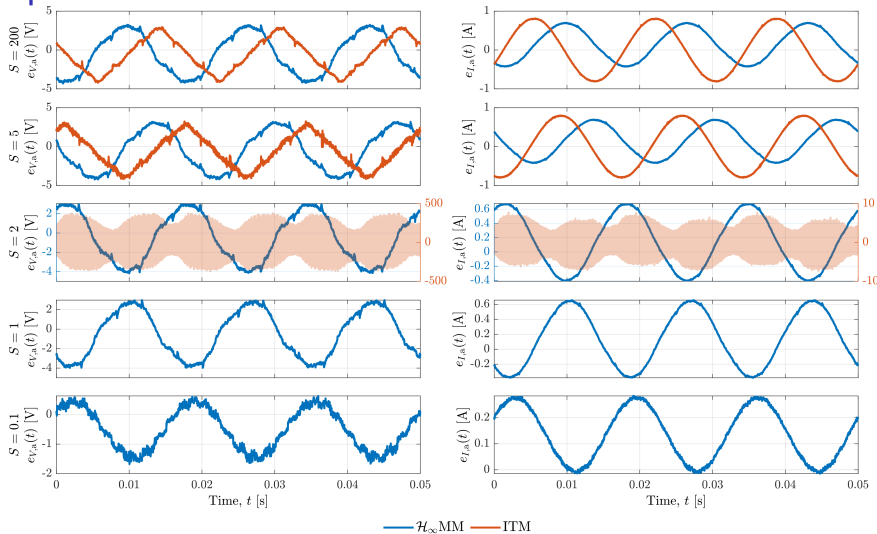
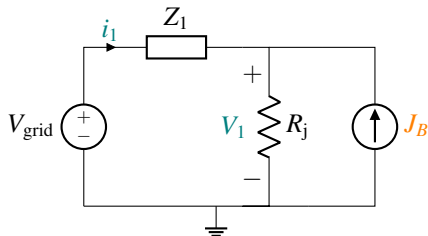
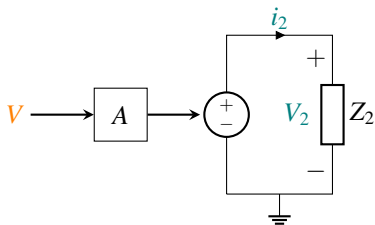


Figure 17: Time-domain response comparison of an $\mathcal{H}_\infty$ model matching-based and ITM-based interface under various operating conditions.

PHIL Model

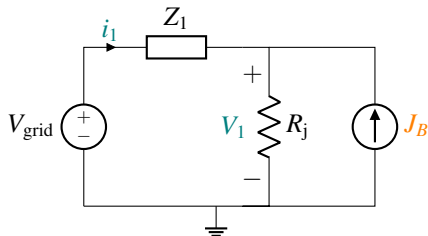


(a) Circuit model of the simulated grid

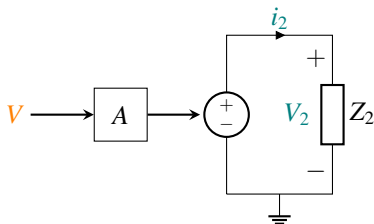


(b) Circuit model of the amplifier and device

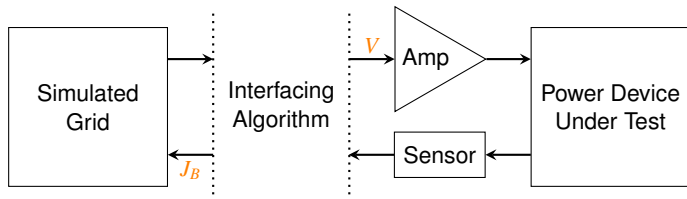
PHIL Model



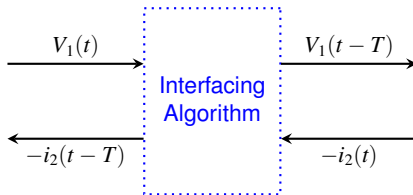
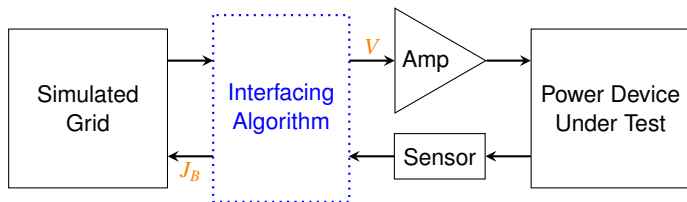
(a) Circuit model of the simulated grid



(b) Circuit model of the amplifier and device

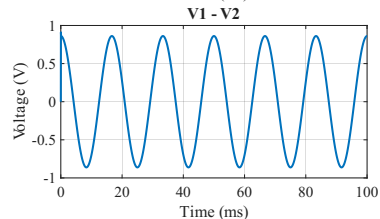
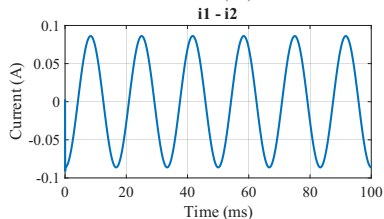
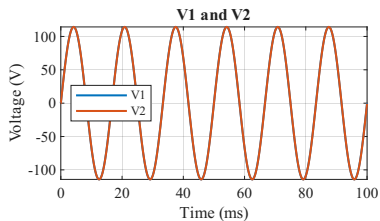
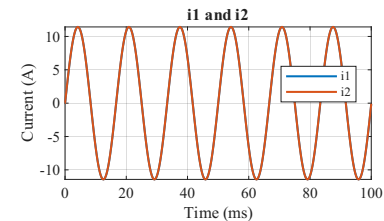


Ideal Transformer Method (ITM)



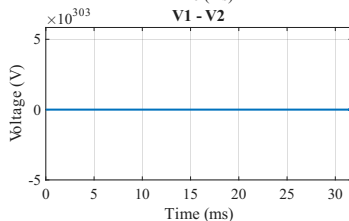
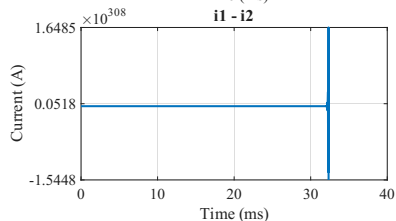
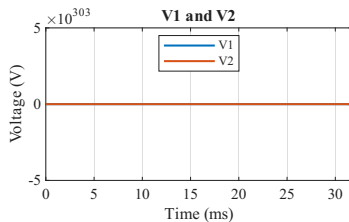
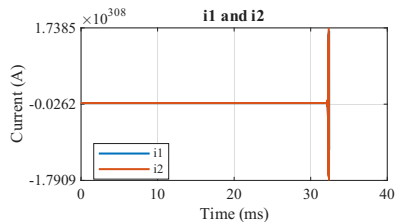
Nominal ITM Response

Response for the ITM Interface

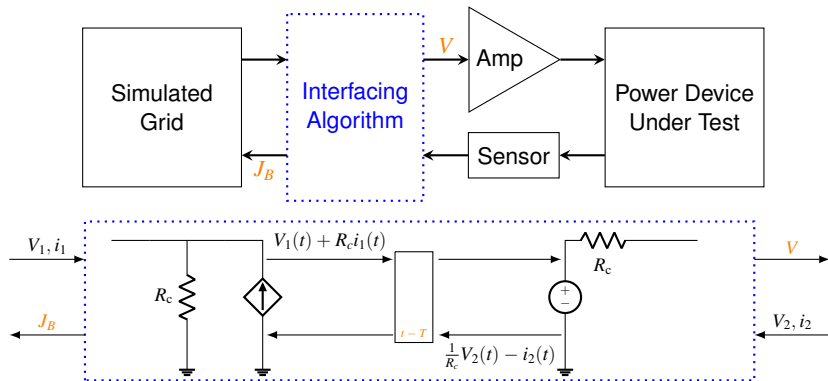


Off-Nominal ITM Response

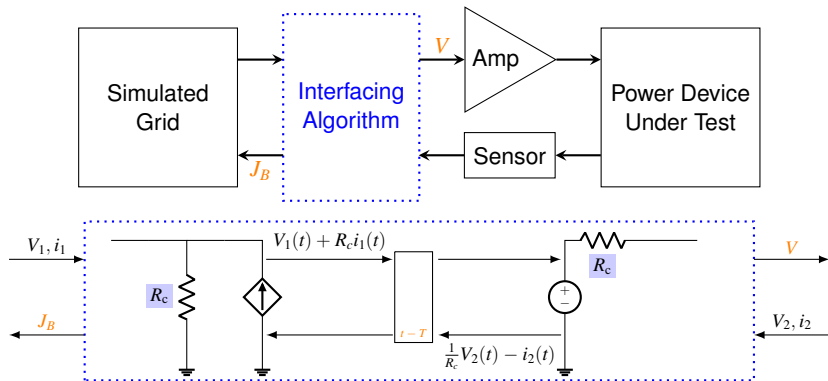
Response for the ITM Interface



Transmission Line Method (TLM)

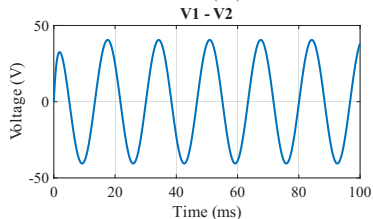
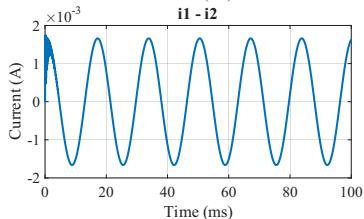
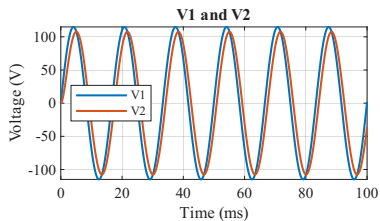
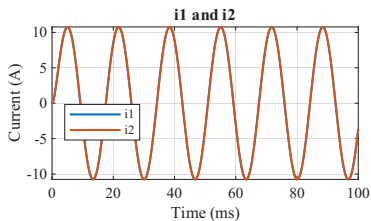


Transmission Line Method (TLM)



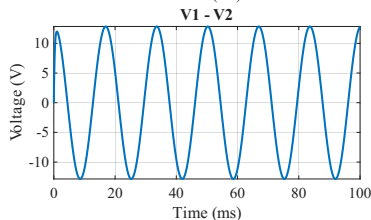
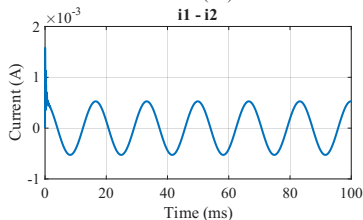
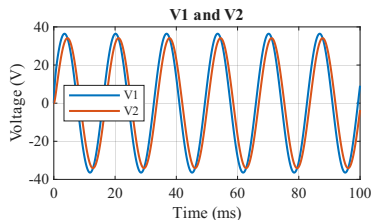
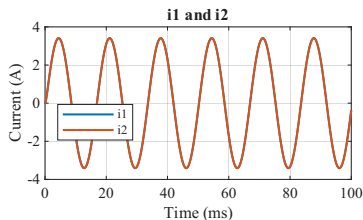
Nominal TLM Response with $R_c = 500\Omega$

Response for the TLM Interface



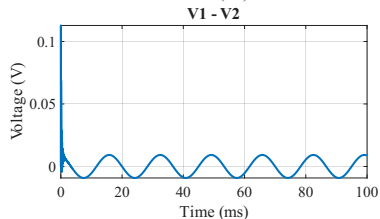
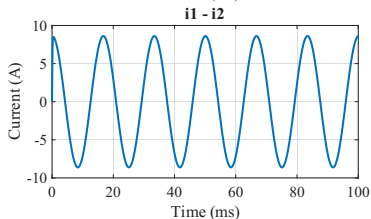
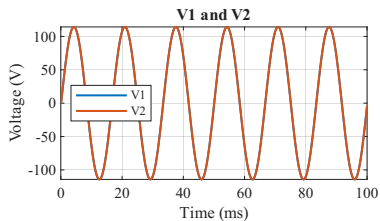
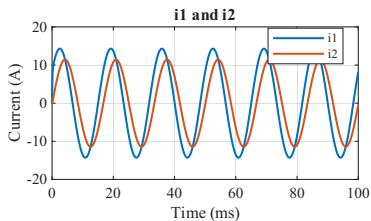
Off-Nominal TLM Response with $R_c = 500\Omega$

Response for the TLM Interface



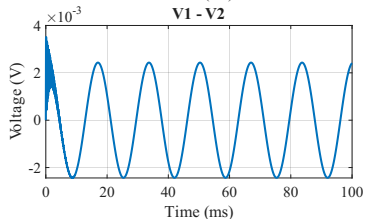
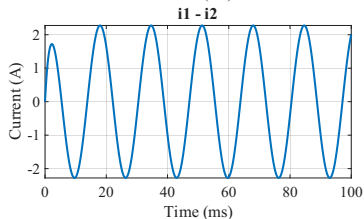
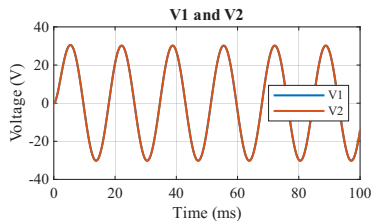
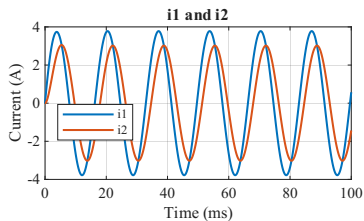
Nominal TLM Response with $R_c = 0.1\Omega$

Response for the TLM Interface



Off-Nominal TLM Response with $R_c = 0.1\Omega$

Response for the TLM Interface



TLM Response

- ▶ The TLM method is useful because it is **PASSIVE!**

TLM Response

- ▶ The TLM method is useful because it is **PASSIVE!**
- ▶ A passive system is one that does not generate energy on its own, but only stores or dissipates energy.

TLM Response

- ▶ The TLM method is useful because it is **PASSIVE**!
- ▶ A passive system is one that does not generate energy on its own, but only stores or dissipates energy.
- ▶ Passive system = stable system.

TLM Response

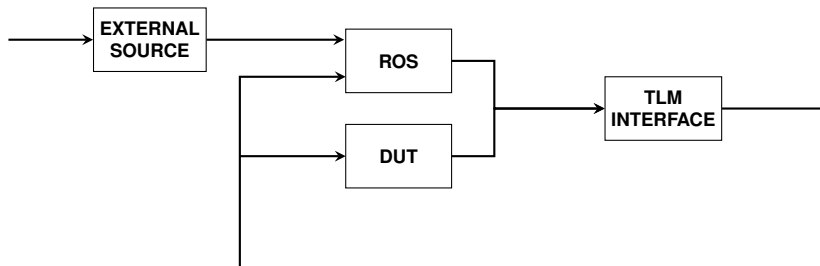
- ▶ The TLM method is useful because it is **PASSIVE!**
- ▶ A passive system is one that does not generate energy on its own, but only stores or dissipates energy.
- ▶ Passive system = stable system.
- ▶ But how can we select R_c to improve performance?

TLM Response

- ▶ The TLM method is useful because it is **PASSIVE**!
- ▶ A passive system is one that does not generate energy on its own, but only stores or dissipates energy.
- ▶ Passive system = stable system.
- ▶ But how can we select R_c to improve performance?
- ▶ New approach: fix the value of R_c and design a feedback controller while perserving passivity.

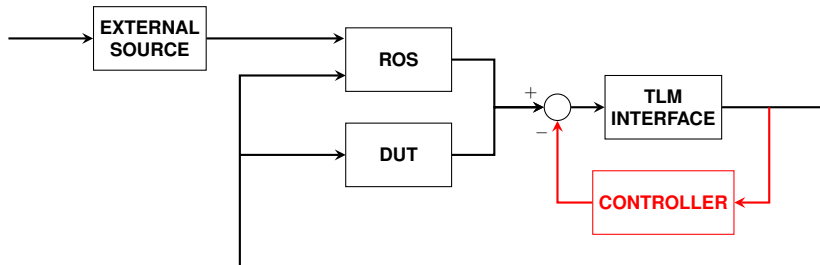
Interconnection of PHIL

- The PHIL problem can be looked at as a block diagram.



Interconnection of PHIL

- Add a controller in feedback.



Controller Synthesis

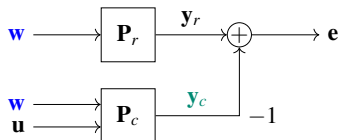
- ▶ The goal of the added controller is to improve the performance for the PHIL interface.

Controller Synthesis

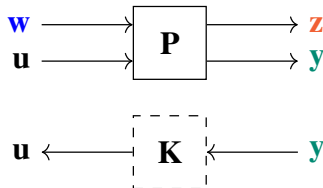
- ▶ The goal of the added controller is to improve the performance for the PHIL interface.
- ▶ This can be done by minimizing the error between signals or through a **model matching** approach.

Controller Synthesis

- ▶ The goal of the added controller is to improve the performance for the PHIL interface.
- ▶ This can be done by minimizing the error between signals or through a **model matching** approach.



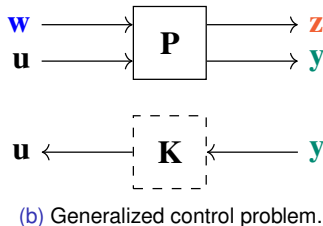
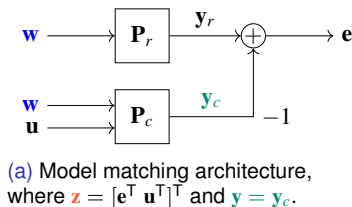
(a) Model matching architecture, where $\mathbf{z} = [\mathbf{e}^T \mathbf{u}^T]^T$ and $\mathbf{y} = \mathbf{y}_c$.



(b) Generalized control problem.

Controller Synthesis

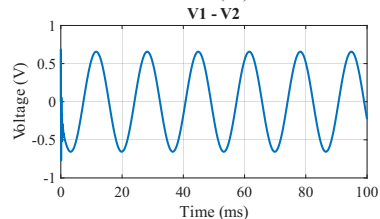
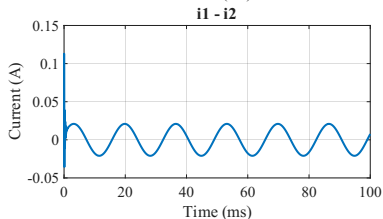
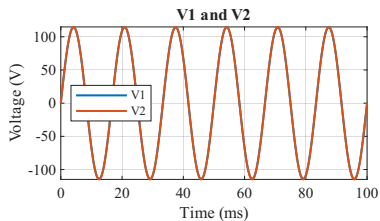
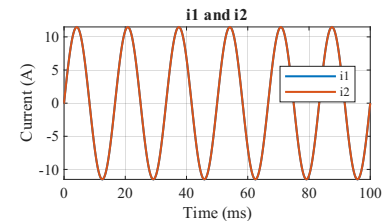
- ▶ The goal of the added controller is to improve the performance for the PHIL interface.
- ▶ This can be done by minimizing the error between signals or through a **model matching** approach.



- ▶ Design a controller using $\mathcal{H}_2$ or $\mathcal{H}_\infty$ synthesis.
- ▶ Add an additional passivity constraint to the controller.

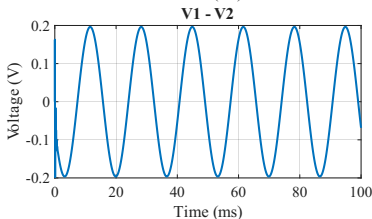
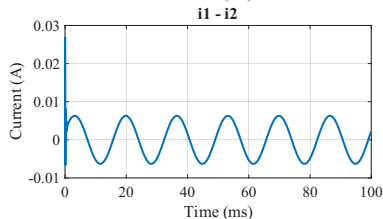
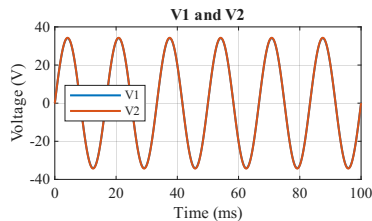
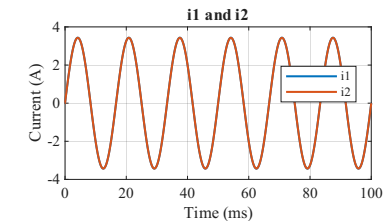
Nominal Response with Passive Feedback

Response for the TLM Interface with SPR Feedback ($R_c = 10\ \Omega$)



Off-Nominal Response with Passive Feedback

Response for the TLM Interface with SPR Feedback ($R_c = 10\ \Omega$)



Conclusion

Conclusion

- ▶ Closed-loop synthesis and testing is a useful approach to PHIL interfacing.

Conclusion

- ▶ Closed-loop synthesis and testing is a useful approach to PHIL interfacing.
- ▶ Model matching and optimal control tools offer a systematic approach to precision.

Conclusion

- ▶ Closed-loop synthesis and testing is a useful approach to PHIL interfacing.
- ▶ Model matching and optimal control tools offer a systematic approach to precision.
- ▶ Optimal passivity-based control improves upon the TLM and the model matching method, offering a systematic approach to both precision and robustness.

References I

- [1] S. Resch, J. Friedrich, T. Wagner, G. Mehlmann, and M. Luther, “Stability Analysis of Power Hardware-in-the-Loop Simulations for Grid Applications,” *Electronics*, vol. 11, no. 1, 2022.
- [2] S. Skogestad and I. Postlethwaite, *Multivariable Feedback Control: Analysis and Design*, 2nd ed. John Wiley & Sons, Inc., 2005.
- [3] W. Ren, M. Steurer, and T. L. Baldwin, “Improve the Stability and the Accuracy of Power Hardware-in-the-Loop Simulation by Selecting Appropriate Interface Algorithms,” in *2007 IEEE/IAS Industrial & Commercial Power Systems Technical Conference*, 2007, pp. 1–7.
- [4] E. Naerum and B. Hannaford, “Global transparency analysis of the Lawrence teleoperator architecture,” in *2009 IEEE International Conference on Robotics and Automation*, 2009, pp. 4344–4349.
- [5] O. Tremblay, H. Fortin-Blanchette, R. Gagnon, and Y. Brissette, “Contribution to stability analysis of power hardware-in-the-loop simulators,” *IET Generation, Transmission & Distribution*, vol. 11, no. 12, pp. 3073–3079, 2017.
- [6] A. von Jouanne, E. Agamloh, and A. Yokochi, “Power Hardware-in-the-Loop (PHIL): A Review to Advance Smart Inverter-Based Grid-Edge Solutions,” *Energies*, vol. 16, no. 2, 2023.

References II

- [7] K. J. Keesman, *System Identification: An Introduction* (Advanced Textbooks in Control and Signal Processing). Springer London, 2011.
- [8] C. Scherer, *Theory of Robust Control*. [Online]. Available: <https://www.imng.uni-stuttgart.de/mst/files/RC.pdf>.