IREQ PHIL System : Closed-Loop Performance of a Megawatt-Scale PHIL Amplifier

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June 17th 2026

Outline

- HQ-PHIL System amplifier topology and key features
- Open/closed loop experimental results
- Hardware key challenges
- Future work/Conclusion

1

(HQ/IREQ) PHIL System amplifier topology and key features

- Overvoltage capacity: 1.5 pu (1 p.u. = 14.4kV RMS)
- Transient output current overload capacity: 10 p.u.
- Effective switching frequency: 32 kHz
- Nominal power : 7.5MW

POWER INTERFACE WITH D.U.T.

Distribution test line 25 kV

Iabc

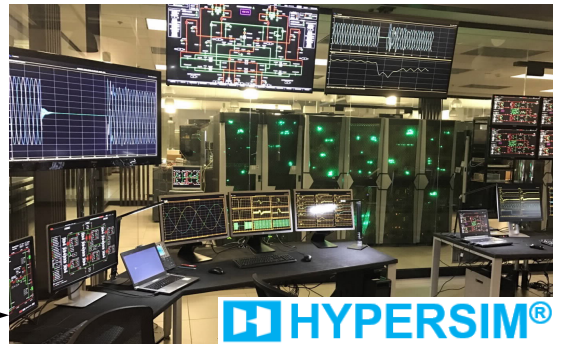
Vabc

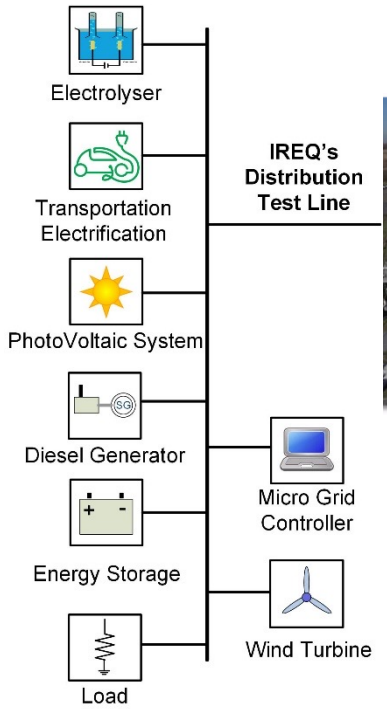
Reference voltage of the amplifier $Vabc_{ref}$

Closed Loop $Iabc_{meas}$

Current measurement to simulator

Real-Time Power System Simulation Lab

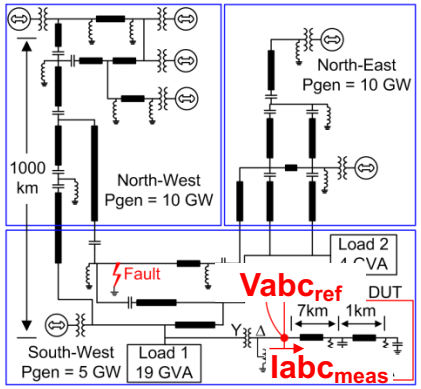




Amplifier powered by the IREQ substation

Amplifier
7.5 MVA @ 25 kV

IREQ Substation 25 kV 60 Hz



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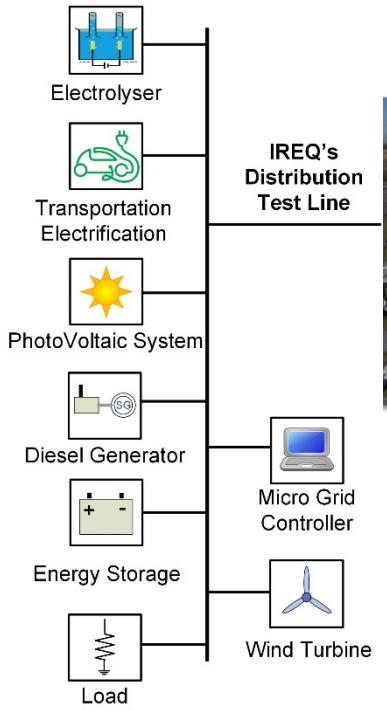
POWER INTERFACE WITH D.U.T.

- High bandwidth (Closed loop stability)
- No output transformer (avoid saturation)
- Scalable (Cascaded H- Bridge)
- Movable (on site D.U.T. testing)
- 3 x single phase (independent arbitrary waveforms on each phase)

SPECIFIC REQUIEREMENTS FOR PHIL



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Amplifier 7.5 MVA @ 25 kV

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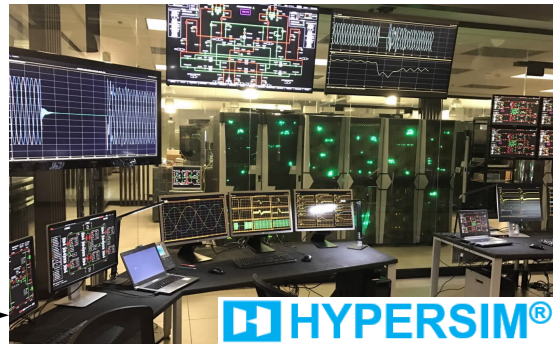

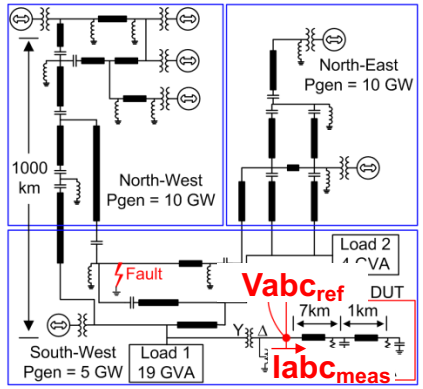

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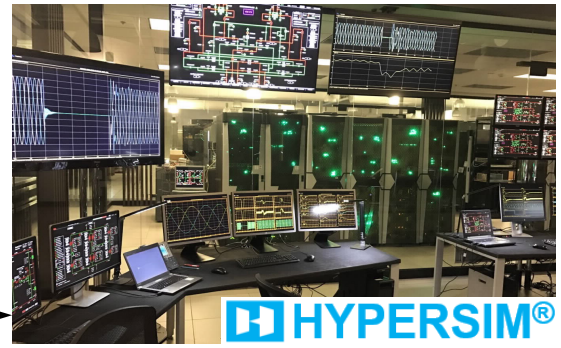
SPECIFIC REQUIEREMENTS FOR PHIL

CONTROL REQUIEREMENTS FOR PHIL

- High-fidelity closed-loop interface
- Designed specifically for PHIL
- Integrated in Hypersim

Real-Time Power System Simulation Lab



Distribution test line 25 kV

Electrolyser
Transportation Electrification
PhotoVoltaic System
Diesel Generator
Energy Storage
Load
IREQ's Distribution Test Line
Micro Grid Controller
Wind Turbine

Iabc

Vabc

Reference voltage of the amplifier $Vabc_{ref}$

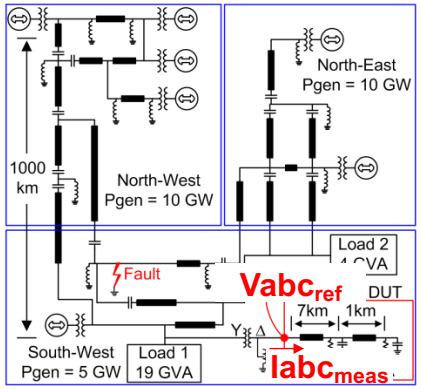
Closed Loop $Iabc_{meas}$

Current measurement to simulator

Amplifier powered by the IREQ substation

IREQ Substation 25 kV 60 Hz

Amplifier 7.5 MVA @ 25 kV



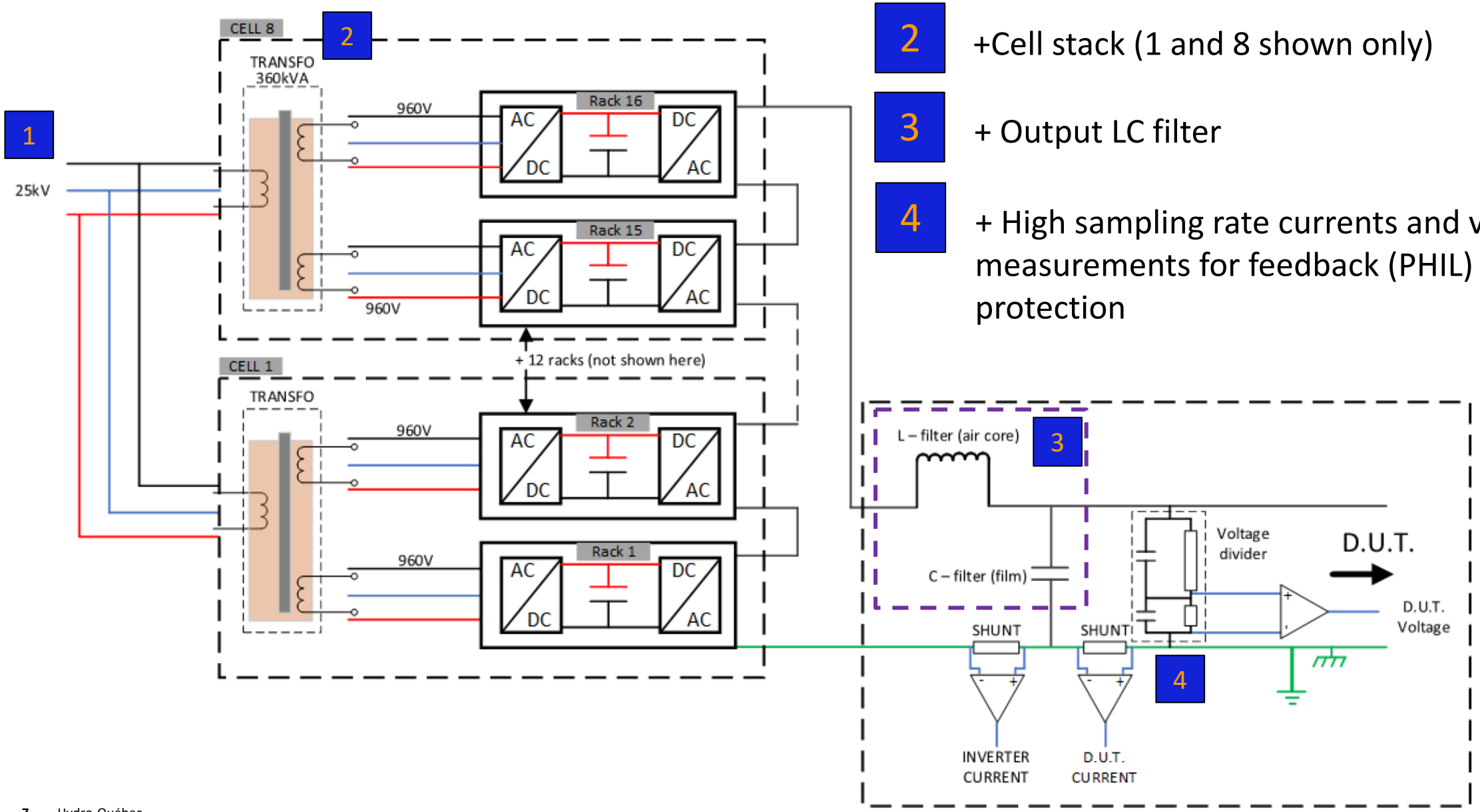
Power amplifier design: topology (complete stack with output measurements)

1 + Amplifier supply (25kV)

2 +Cell stack (1 and 8 shown only)

3 + Output LC filter

4 + High sampling rate currents and voltage measurements for feedback (PHIL) and protection



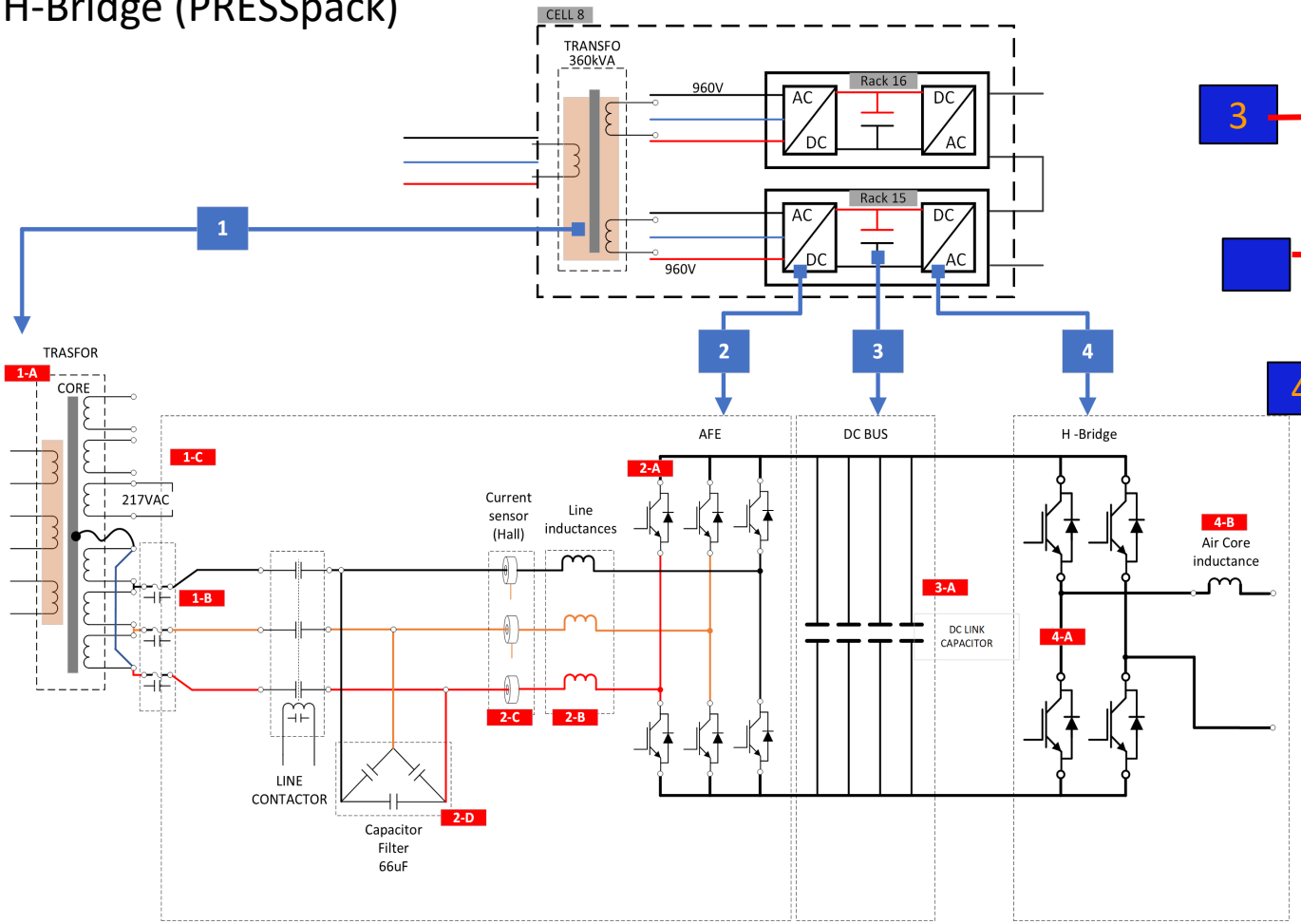
Power amplifier design: CHB topology (power cell structure)

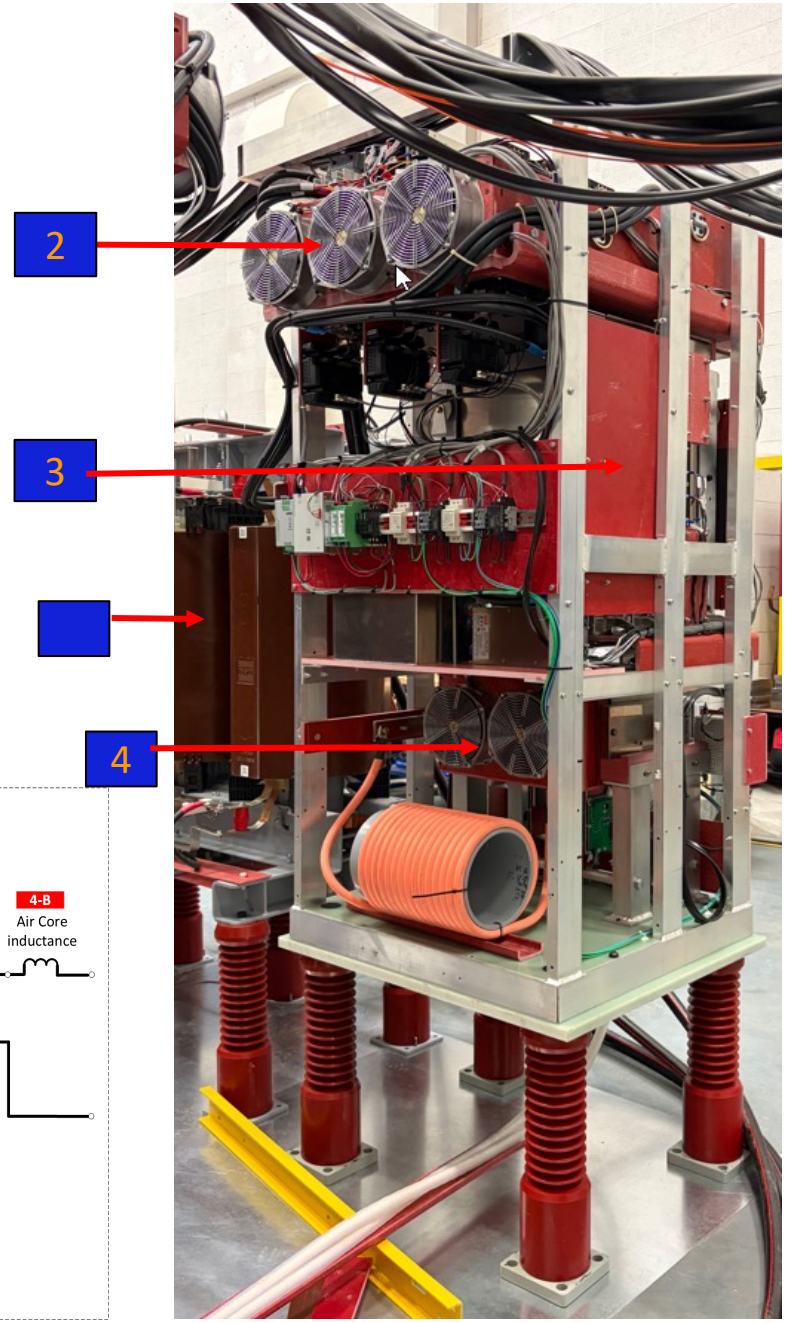
1 + 25kV/960V 360kVA Transformer

2 + 180kVA AC/DC Active Front End (AFE)

3 + High energy 2kV, 14mF capacitor bank

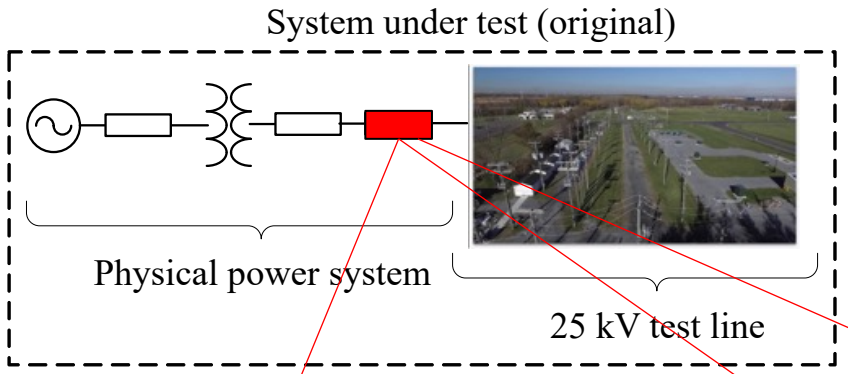
4 + Output H-Bridge (PRESSpack)





High-fidelity closed-loop interface for EMT-type PHIL

Stable real-time decoupling remains a critical challenge in EMT-based PHIL systems



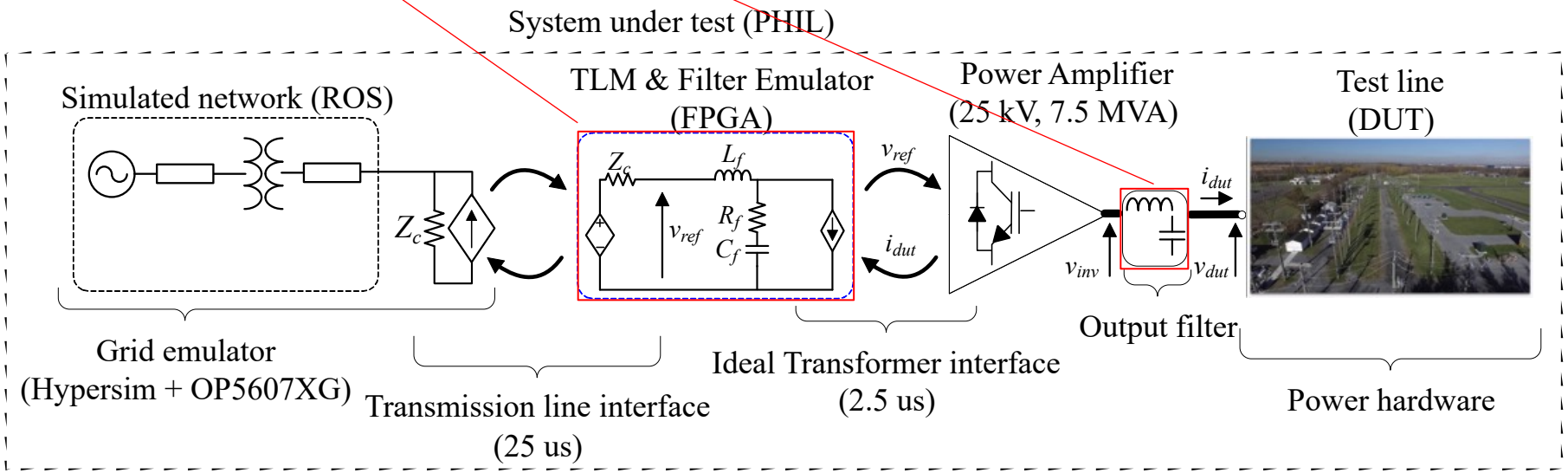
A **TLM-based interface algorithm** (IA) was successfully deployed between the EMT simulator and the power amplifier

Seamless transfer from grid emulation to load emulation

This IA relies on a dual feedback-loop architecture:

- CPU–FPGA (TLM): **inherently stable interface**
- FPGA–Power Amplifier (ITM): **highly stable** thanks to the fast control loop, but requiring a high-bandwidth power amplifier

A part of a transmission line already existing in the power system is used to represent the TLM-IA and PA output filter



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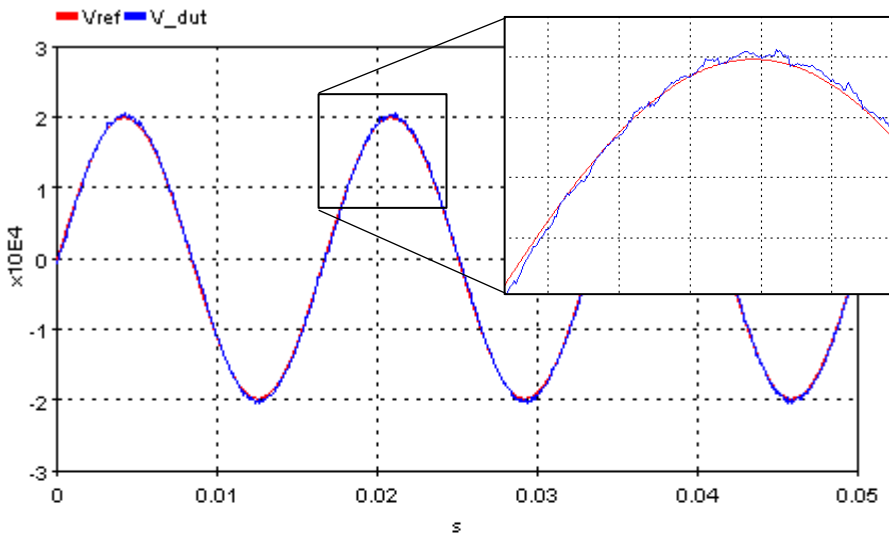
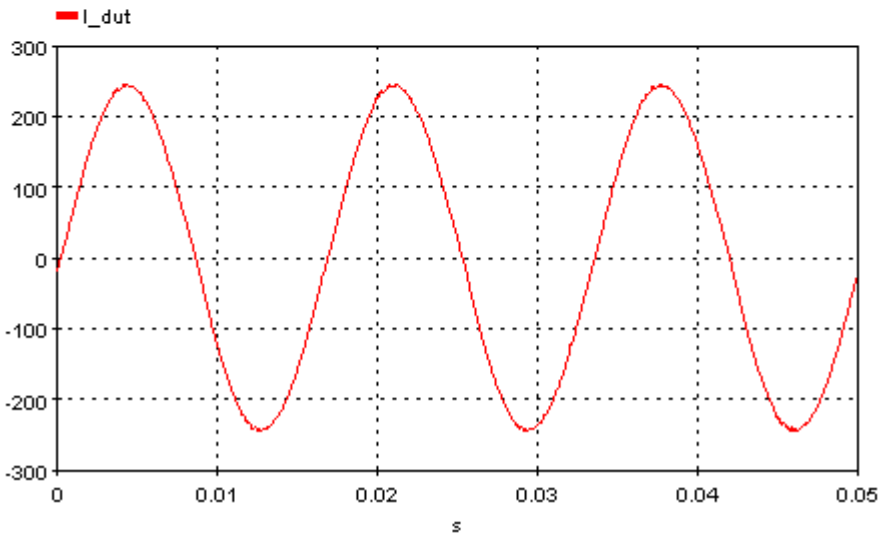
Open/closed loop experimental results

(preliminary results)

Open loop experimental results

2.6 MW resistive load operated at full power

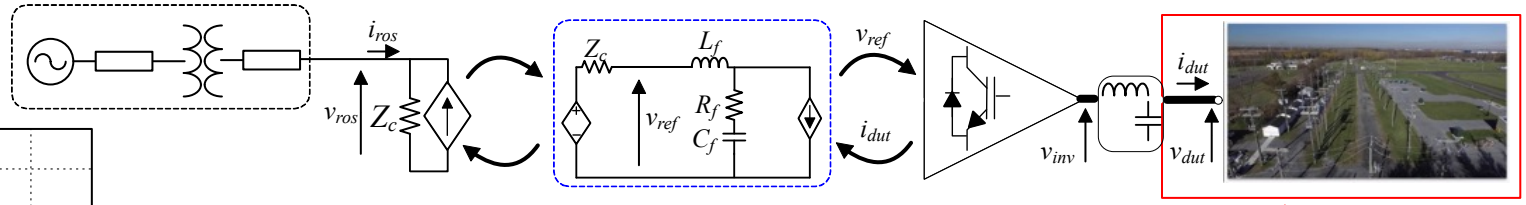


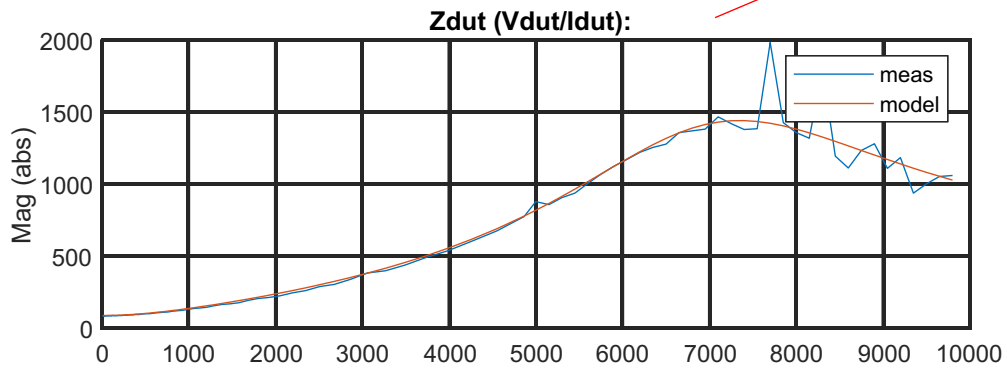


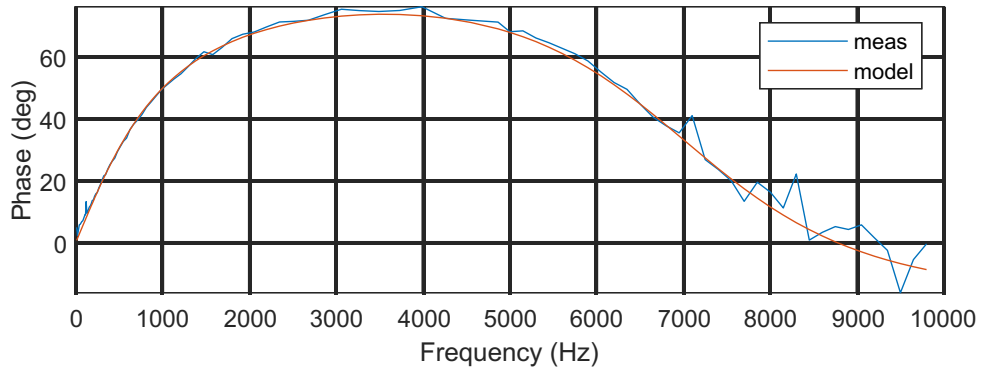
THD (< 6kHz)
- 0,97 % (V)
- 1,27 % (I)

THD (< 60kHz)
- 1,4 % (V)
- 1,34 % (I)

2.6 MW resistive load
(behind line and transformer)

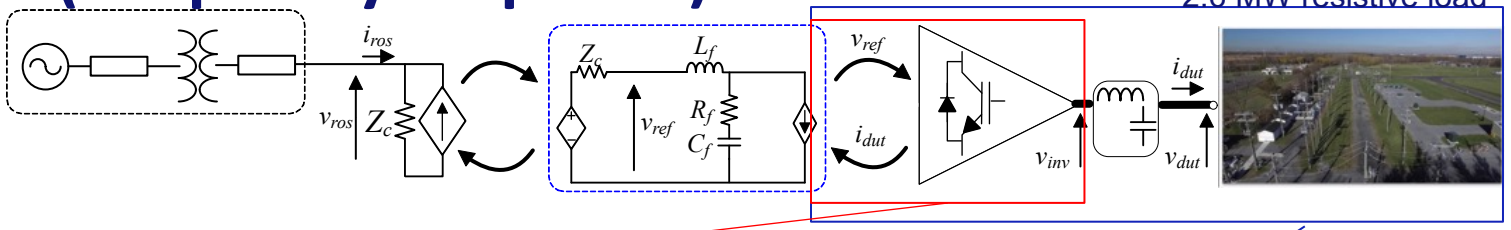


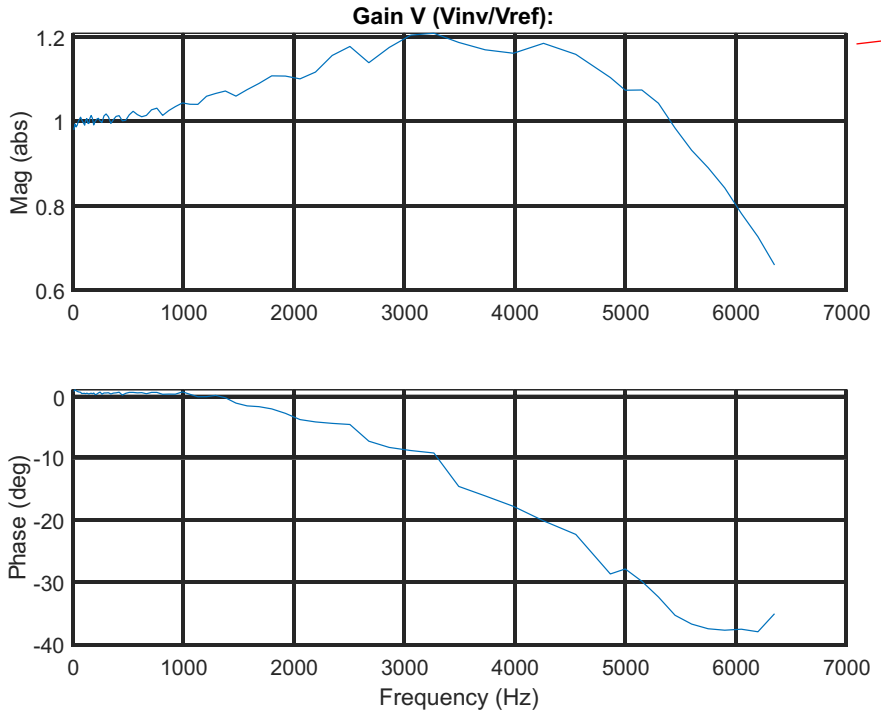




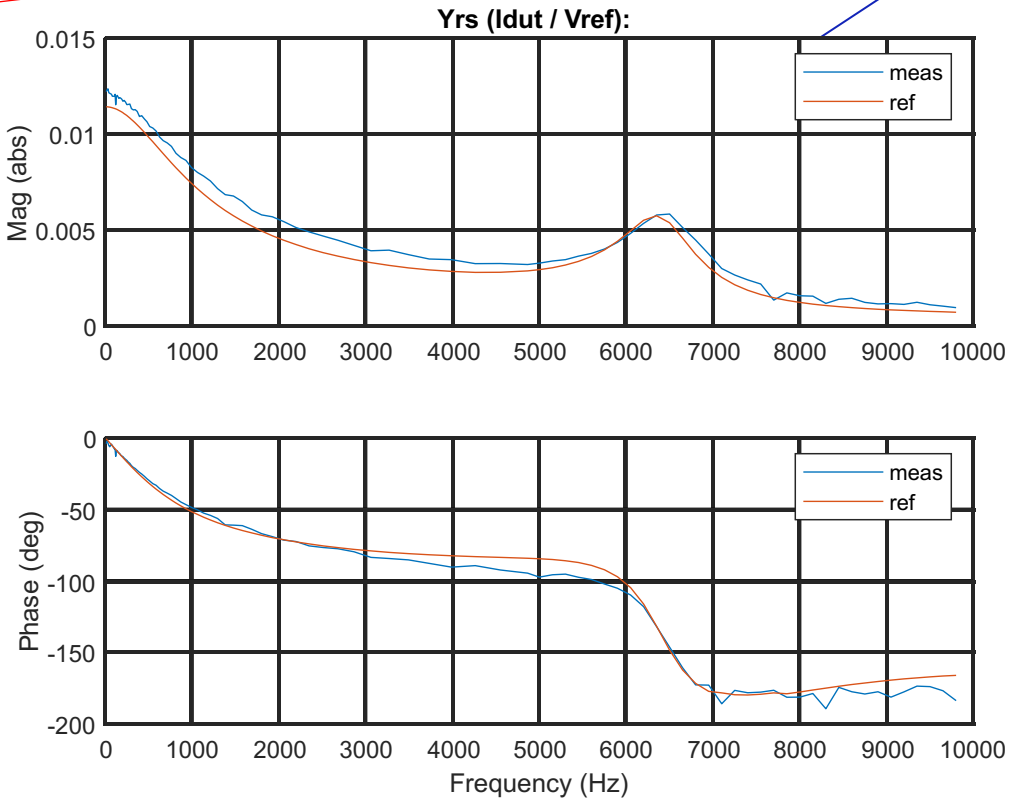
We fitted a model of the DUT for the next performance analysis

Open loop experimental results (frequency response)



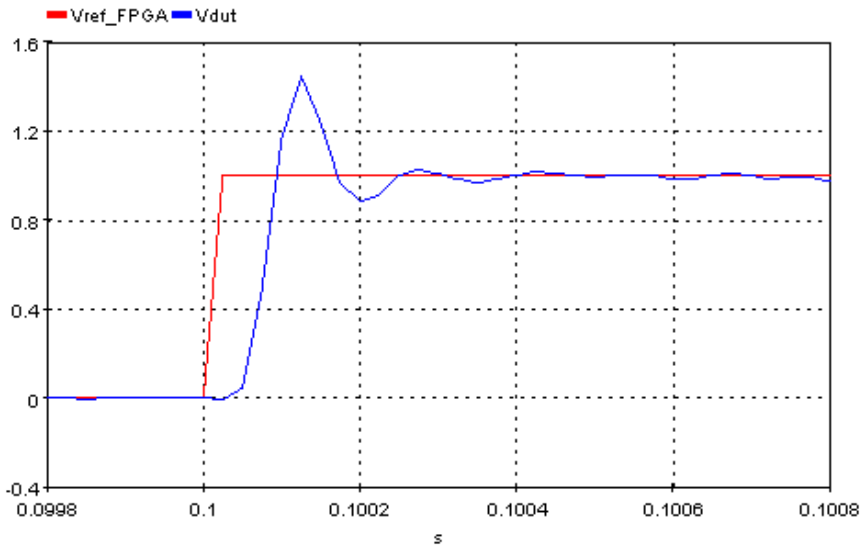


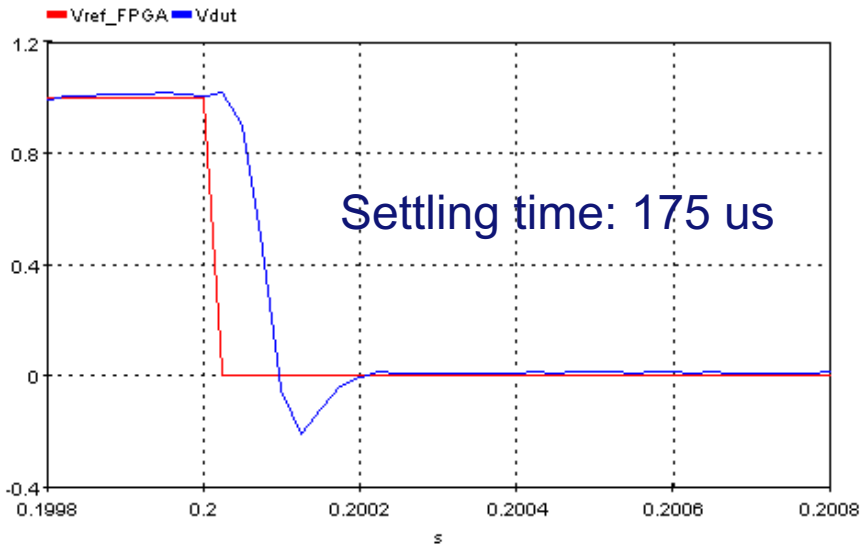
Open-loop bandwidth: 6 kHz



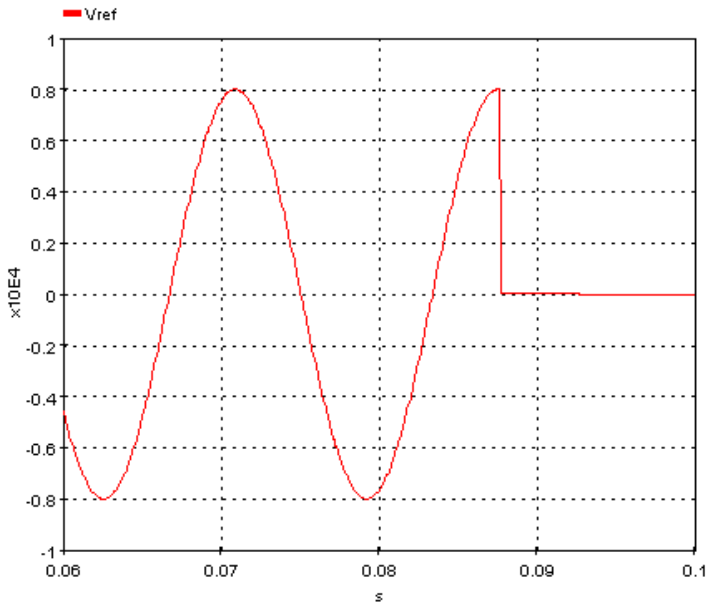
Open-loop feedback delay: ~15 us
(at nominal current)

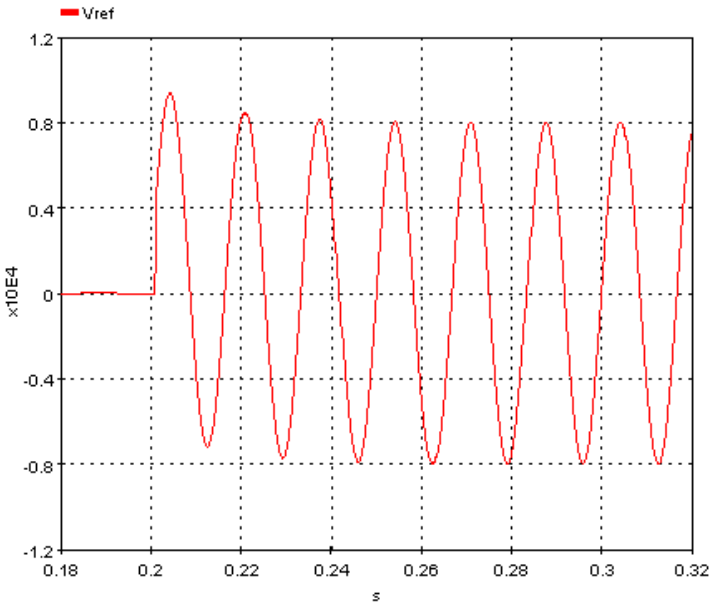
Open-loop dynamic performance

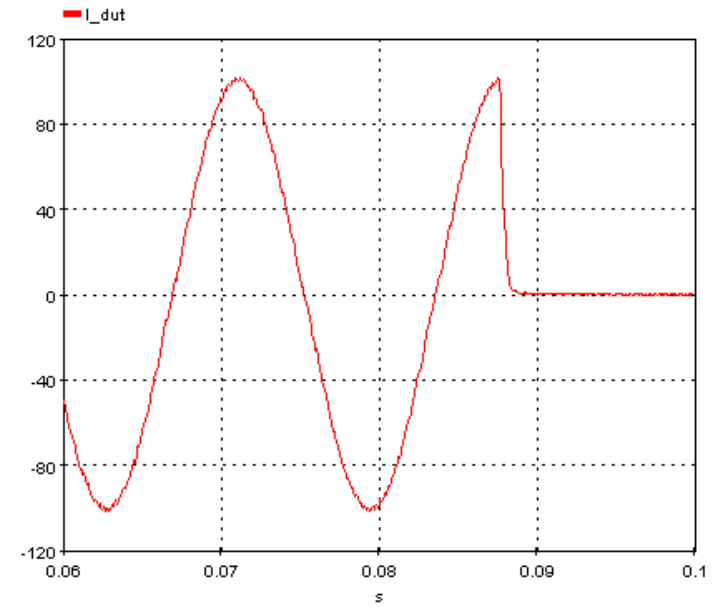


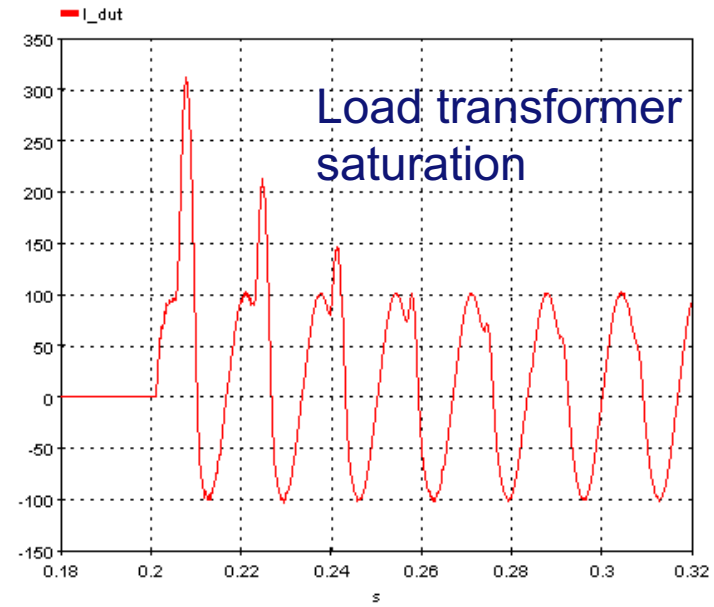


Zero voltage ride-through (Test line 2.6 MW load)

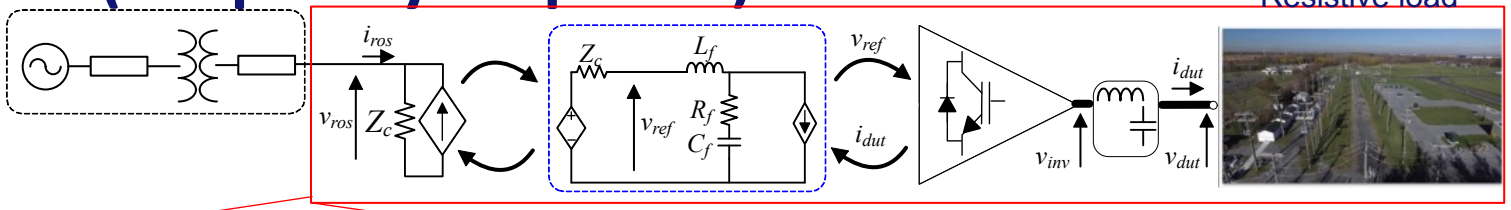




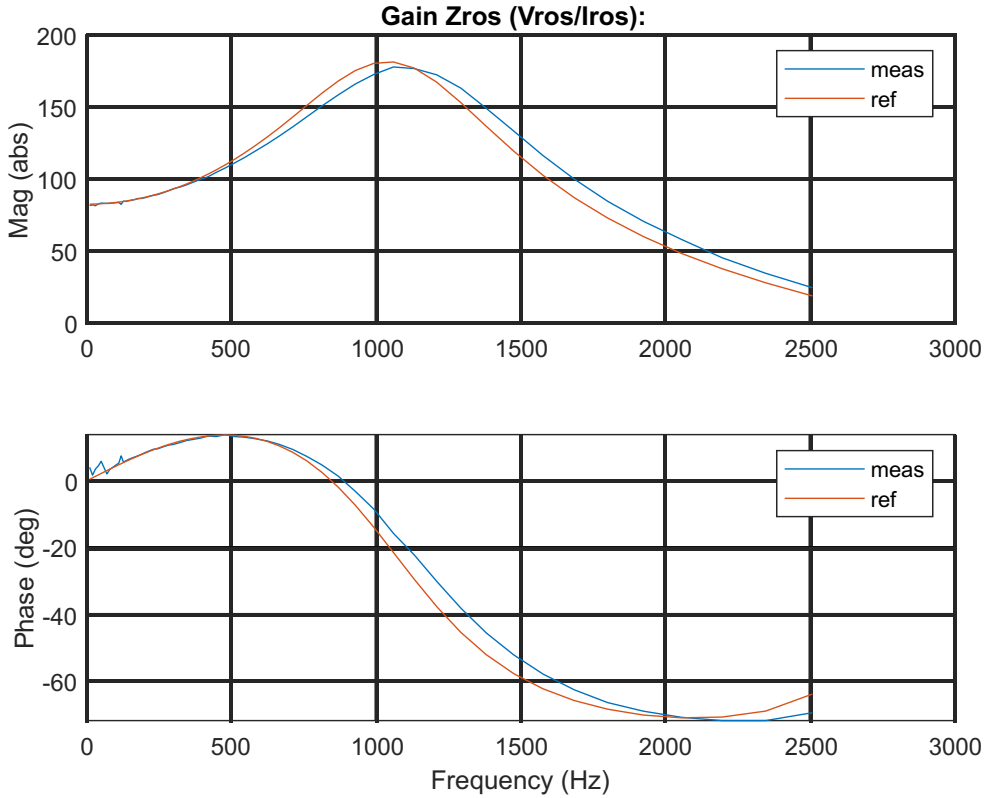




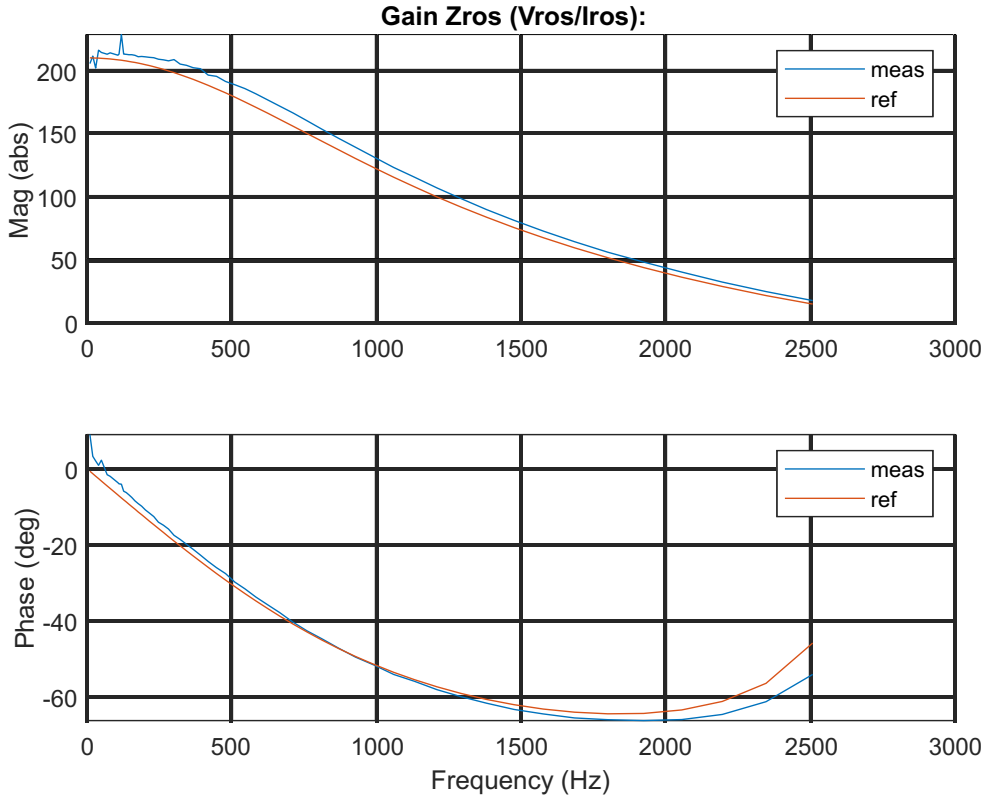
Closed-loop experimental results (frequency response)



2.6 MW resistive load

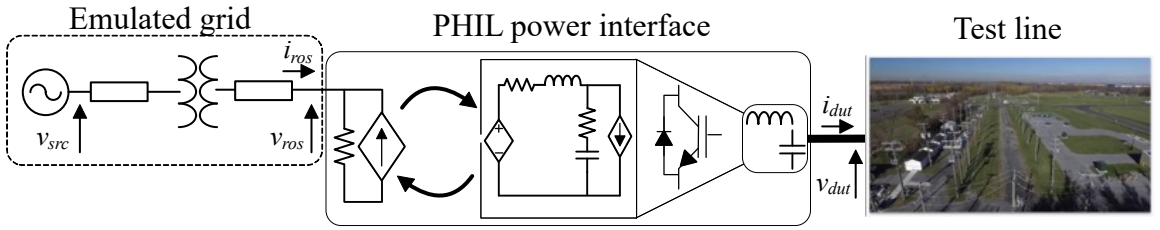


1 MW resistive load

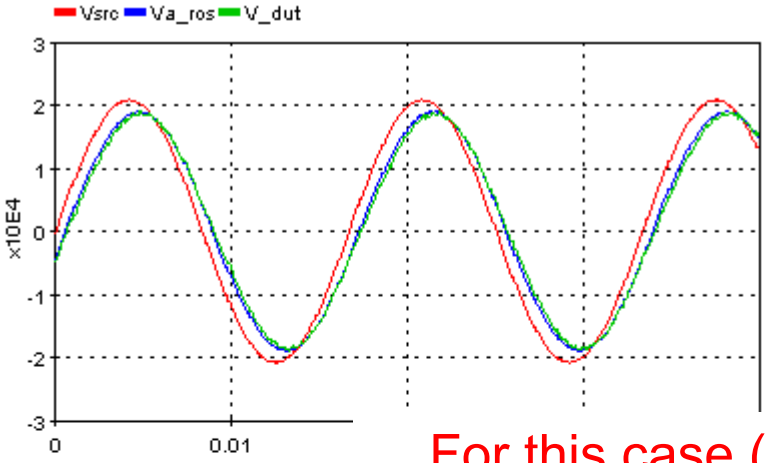


Stable and accurate closed-loop PHIL

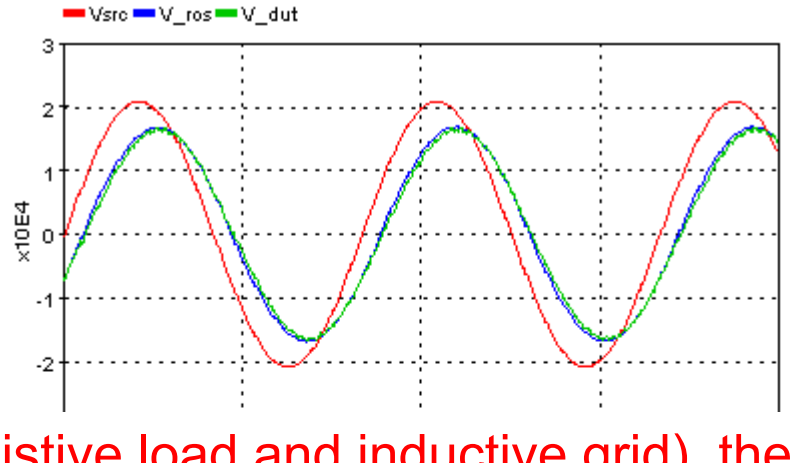
Closed-loop experimental results (weak grid)



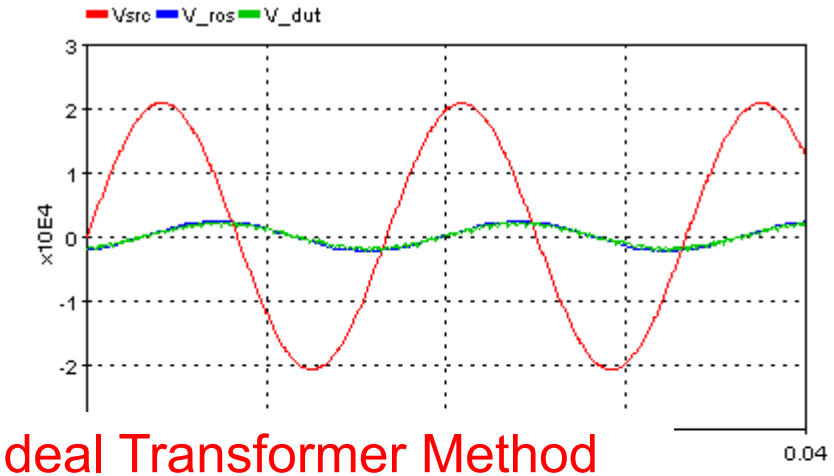
SCR = 4, X/R = 4



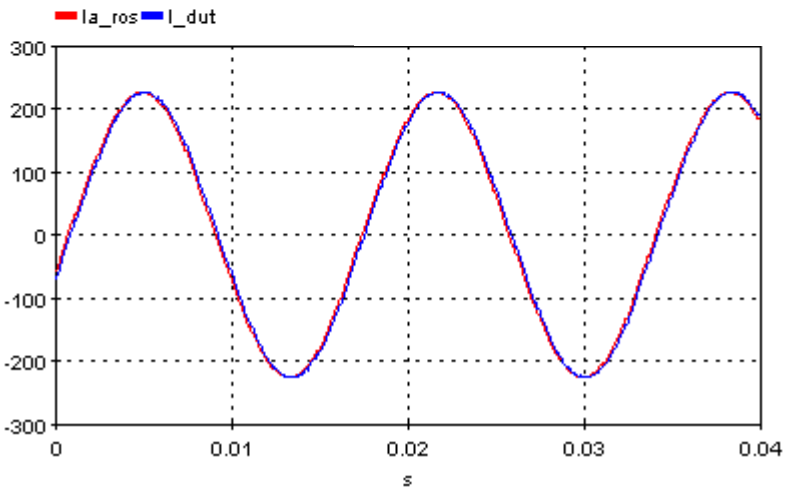
SCR = 2, X/R = 4

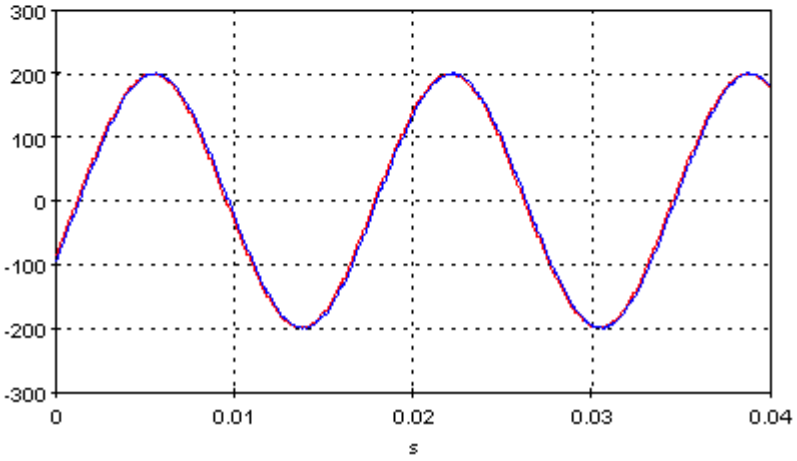


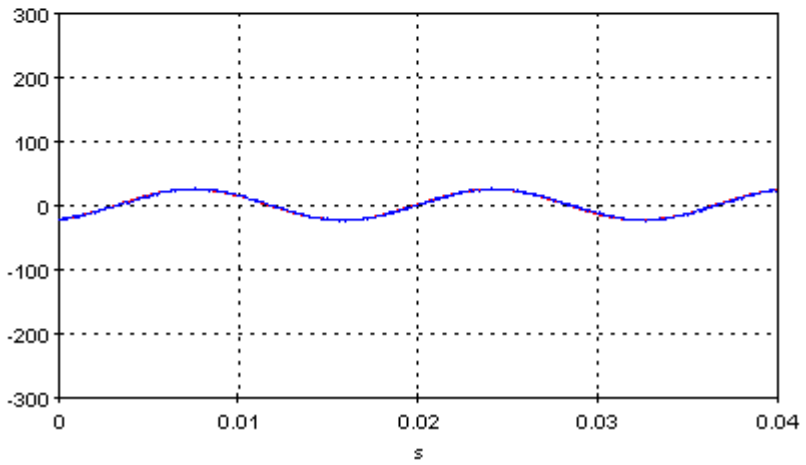
SCR = 0.1, X/R = 4



For this case (resistive load and inductive grid), the Ideal Transformer Method becomes **unstable** for SCR values below 20!





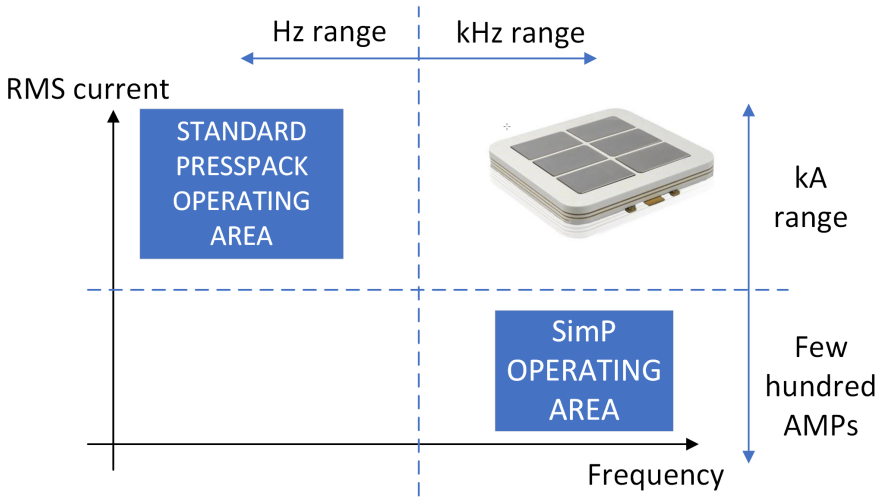


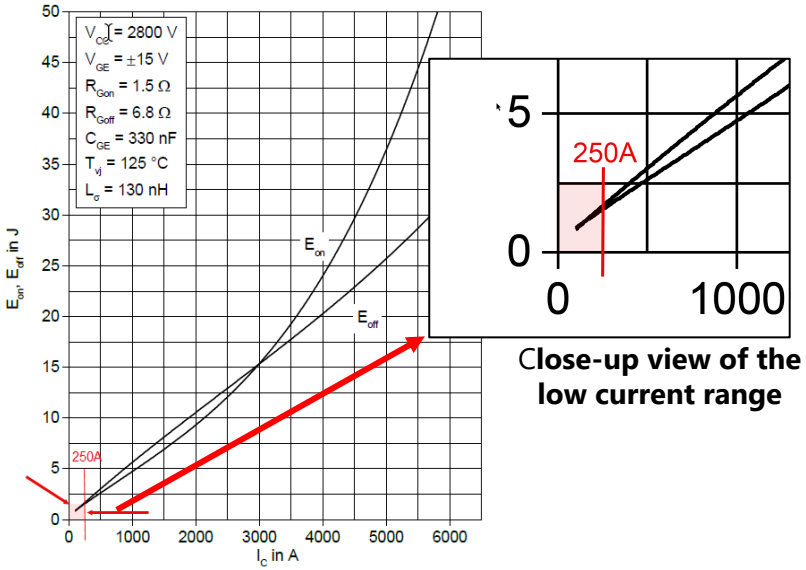
3

HARDWARE CHALLENGES

Interesting Hardware Challenges : Out of specs

- **Out of specs IGBT presspack operation**
  - **Why PressPACK?** : Usually used in serial topologies to avoid open circuits in operation (risk of arcing, uncontrolled shut down)
  - **PressPACK IGBT** : designed for low switching frequencies and high currents
  - **Current constraints (SimP)** : Low currents in normal operation – high current to emulate short circuit conditions for 1 second
  - **Switching frequency (SimP)** : Low frequency for interconnexion – high frequency (1kHz) in SimP to synthesize the waveform with a low THD and optimize the bandwidth
  - **Impacts**
    - Always out of specs in datasheet : extrapolation is needed + extra measurement in the lab to cover this operating range





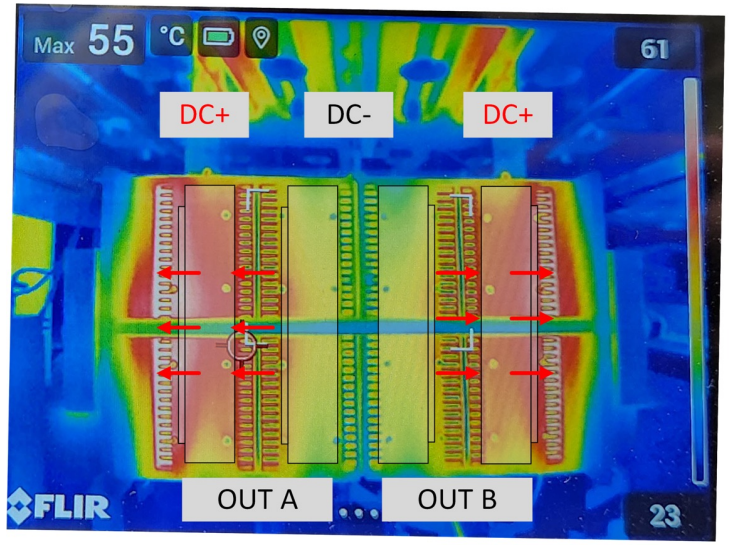
Close-up view of the low current range

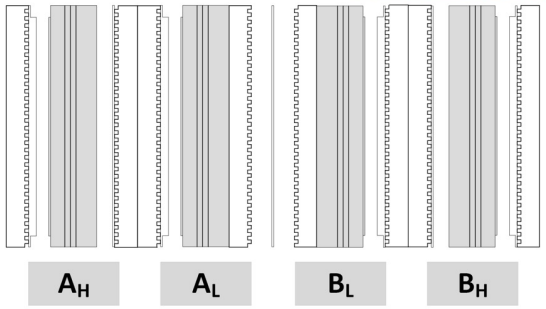
Turn ON and Turn OFF energy

Hardware Challenges (Thermal management)

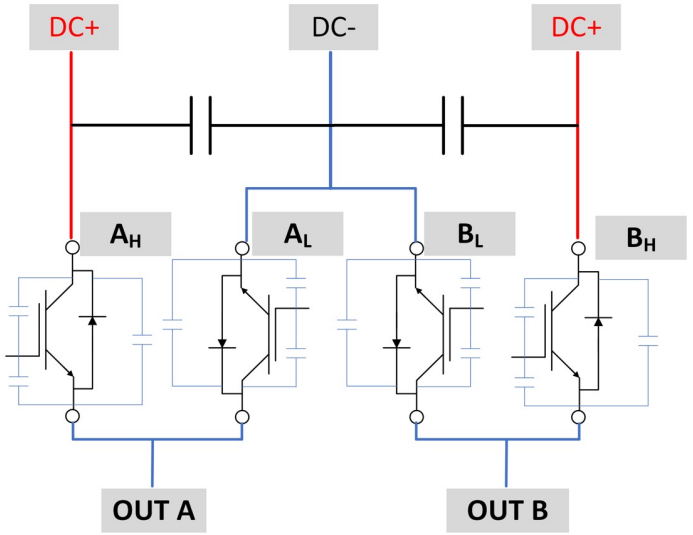
- **Air cooled thermal management challenges**
  - PressPACK IGBT are dissipating high power at high switching frequency with an asymmetrical heat transfer
  - Air cooled strategy has been selected for many considerations
    - (+) Environmental (no cooling liquid spill even under any type of failure)
    - (+) ease of cell replacement (no complex cooling system to connect/disconnect)

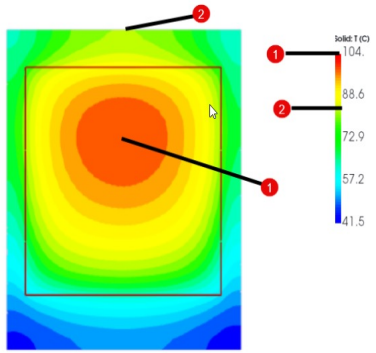
  Downside
    - (-) high power density losses must be extracted with limited cooling -> heat flow must be studied carefully





H bridge temperature distribution under full power operation

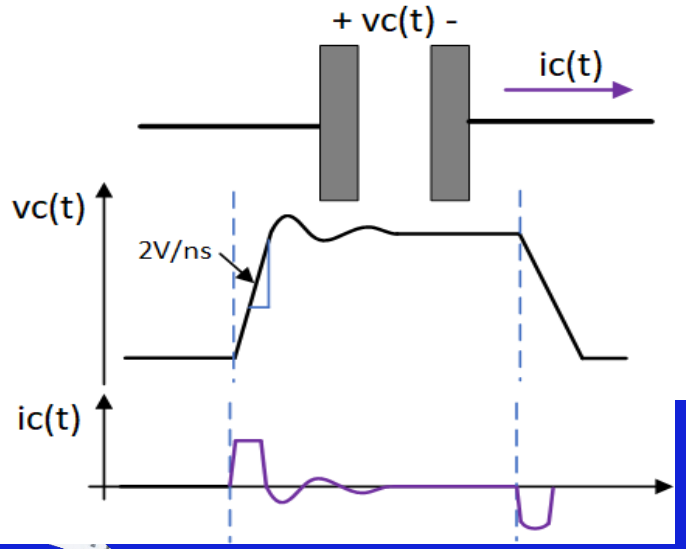


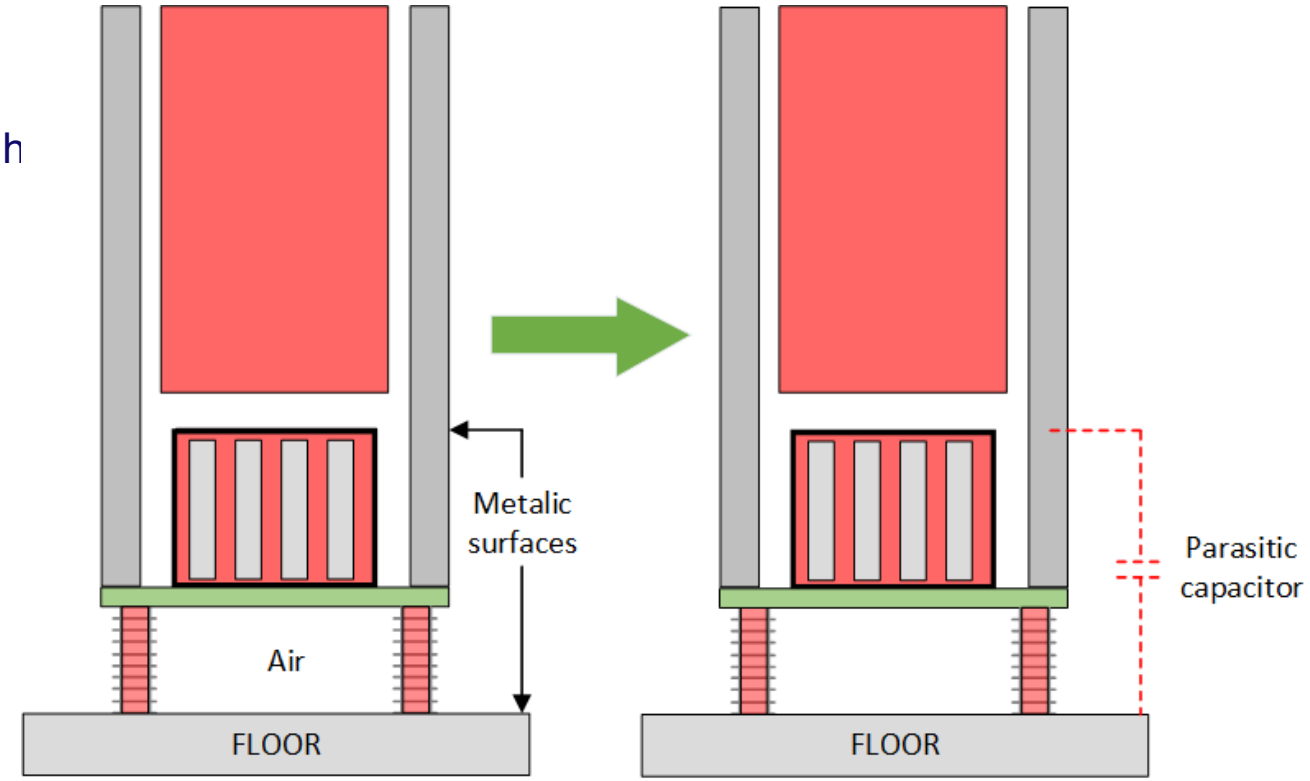


Temperature distribution study with FEM

Basics to appreciate the Following challenge

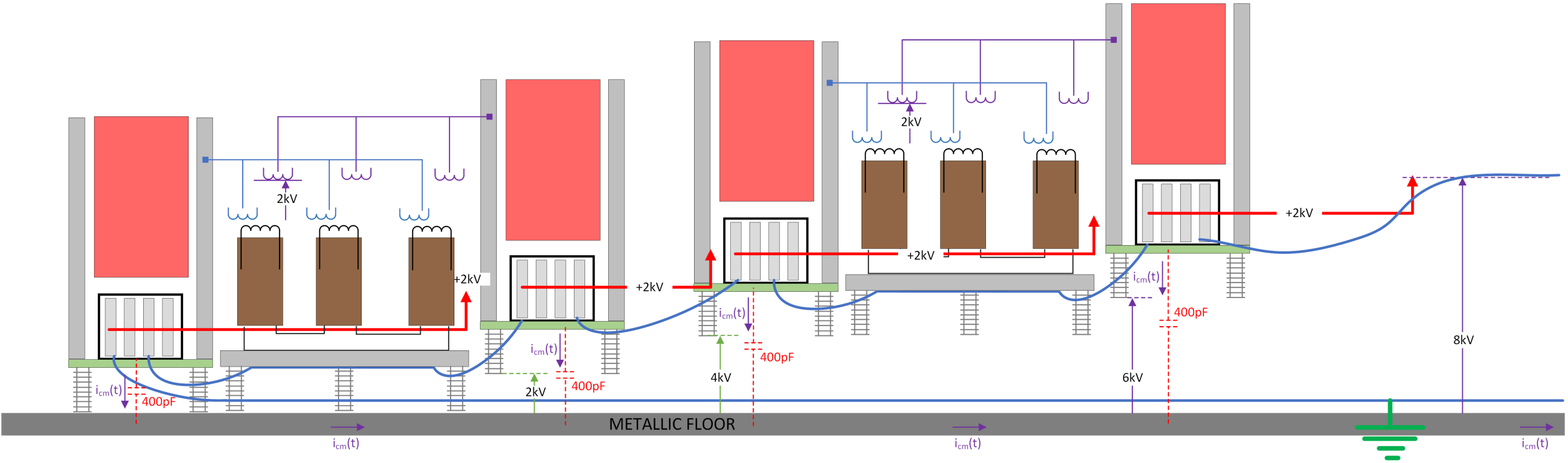
- **Common mode is a particularly important concept in power conversion**
  - Three concepts are important to understand to appreciate the last challenge (for today)
    - Common mode noise is generated by sharp voltage variation and ring at turn off (cause by IGBT switching)
    - Common mode travel by displacement currents (through invisible parasitic capacitors)
    - Parasitic capacitor are formed by two metallic surfaces separated by an isolation (air in the present case)





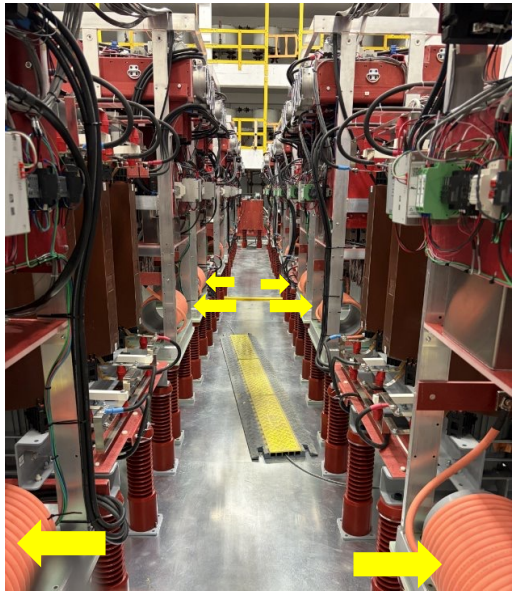
Hardware Challenges (Common mode currents)

- **The staircase voltage effect in cascaded H-bridge converters**
  - When the H-bridge switches, cell voltages rise and fall (with respect to the floor) at fast rate, generating common mode currents circulating from racks to the floor.
    - These common mode current are circulating in the D.U.T.

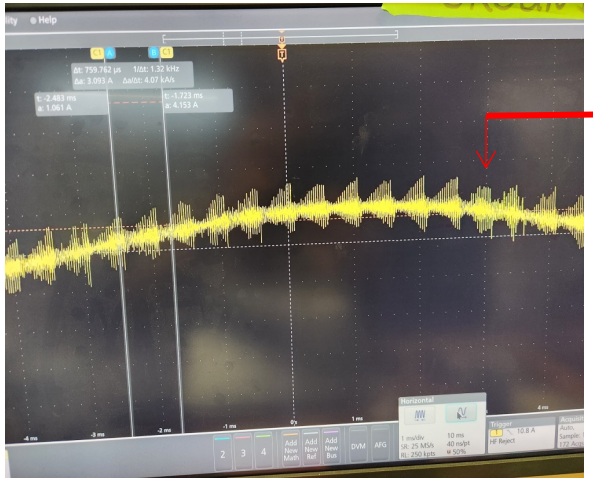


Hardware Challenges (Common mode curent)

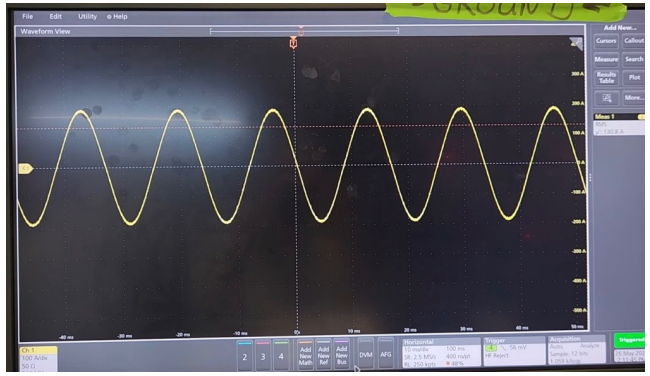
Lumped filter inductance



Distributed filter inductance



Load current with lumped filter inductance



Load current with distributed filter inductance

- **Common mode currents in the load**
  - 16 current spikes during 1 switching cycle of the H-bridge
    - Seems to be a spatial effect (where the rack is located, relative to the load connection)

Conclusion + Future work

- **Conclusion**
- Integrated design fully dedicated to the application (algorithm, amplifier, etc.)
- Performance exceeds expectations, particularly for a system at this power and voltage levels.
- The extended closed-loop concept (low SCR) has been experimentally validated and is functional.

- **Future work**
- Fine tune the calibration of the measurement system
- Dynamic dead-time compensation
- Filter active damping
- Integration in the containers

Thank you ! Questions?